AD41240
A quad 12 bit-40 Ms/s 450 mW CMOS A/D Converter

FEATURES

- Four channels, 12 bit 40 Ms/s ADC
  - Possibility of operating as single 14 bit, 40 Ms/s ADC.
- LVDS output buses
- Power consumption: < 450 mW with all channels active
- Input:
  - differential +- 450 mV
  - Vcm is VDD/2
- Reference clock input:
  - LVDS
- Package: 1 mm pitch BGA
- 144 pins, 13x13 mm, 1.7 mm height
- Single supply voltage: 2.5V
- Low latency
- Radiation tolerant, 0.25 μm CMOS technology

PRODUCT DESCRIPTION

The AD41240 is a CMOS, 450 mW, quadruple 12-bit, 40 MSPS analog-to digital converter designed especially for the needs of the CMS electromagnetic calorimeter, but also compatible with many other application. The AD41240 has a multistage pipelined architecture with output error correction logic; the AD41240 offers accurate performance and guarantees no missing codes over the full operating temperature range. Selected channels in the AD41240 can be placed into a standby mode of operation reducing considerably the power consumption. The AD41240's digital I/O interfaces to LVDS logic for all the high speed inputs and outputs signals and to CMOS 2.5V compatible logic for all configuration pins.

The AD41240 comes in a space saving 144-balls fine-pitch Ball Grid Array and is specified over the commercial (-10°C to +70°C) temperature range.

PRODUCT HIGHLIGHTS

Low Power

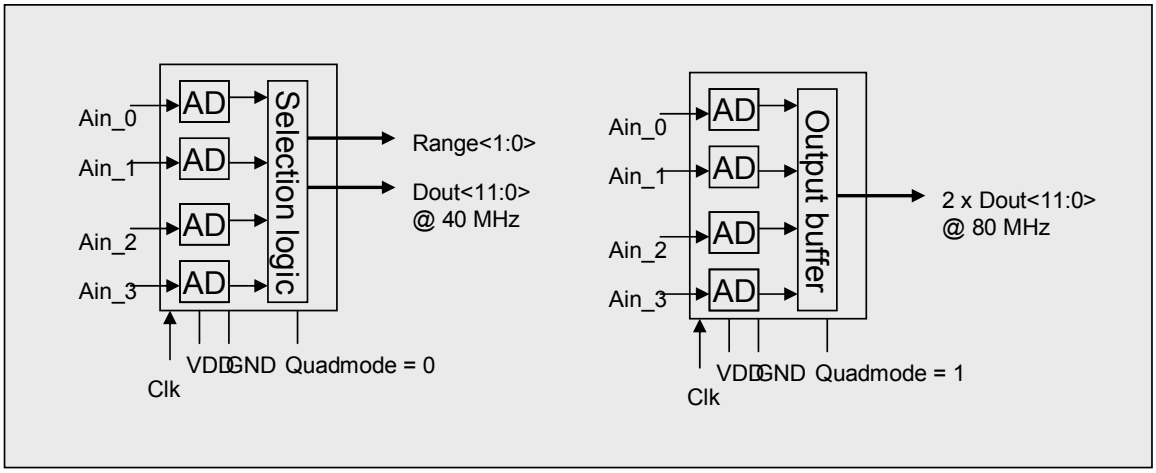
The AD41240 consumes only about 450 mW when all four channels are used. Unused channels can be put in a very low power stand-by mode by using the ENADC<3:0> configuration pins. For example, disabling two unused ADCs can reduce the total power consumption by almost a full factor of two.

Operating Modes

The AD41240 can be used in a variety of modes, essentially defining the width, protocol and speed of operation of the output bus.

The different operating modes can be selected using the MODE<2:0> configuration pins. The modes are summarized in the table below:

Mode	Description	Speed [MHz]	Width
0	Quad ADC	80 DDR	2x12
1	Ecal Direct	40	1x14
2	Ecal with Hyst	40	1x14
3	Ecal Direct	80 DDR	1x7
4	Ecal with Hyst	80 DDR	1x7
5	Transparent (0-1)	40	2x12
6	Transparent (2-3)	40	2x12
7	Invalid		



For low noise generation. the output data bus uses LVDS signaling, therefore each bus lines uses two pins.

In mode 0 the AD41240 behaves as a four independent analog to digital converters sharing a common output bus. The output bus outputs data in a Double Data Rate fashion, with two ADCs being multiplexed on the same bus and two buses of 12 bits being used. Data is output on the two different clock phases.

In mode 1 the AD41240 behaves as a single ADC as required by the CMS ecal system. It is assumed that when used in this mode the ADC input is generated by four amplifiers with different but overlapping gains connected to the same input signal (see for example Figure 1). This configuration allows to expand the dynamic range on which a signal is sampled by maintaining the same actual resolution and speed.

In this mode the so called "selection logic block" brings to the output bus the data from the first ADC that is not saturated. Saturation is defined as having a converted value with the 8 most significant bits all equal to '1'. The least significant channel is channel 0 and the most significant channel is channel 3. When the AD41240 is connected to four input amplifiers having a gain of respectively 8, 4, 2 and 1 it then behaves as a 14 bit 40 Ms/s ADC. In this mode the output bus is 14 bit wide, with the two MSBs indicating which channel has been selected and the 12 LSB indicating the value digitized by the corresponding ADC. The output data rate is 40 MHz.

Mode 3 is identical to mode 1, apart from the fact that the output bus is configured to run only on 7 bits but at double data rate mode, i.e. at 80 MHz.

Mode 2 behaves also as mode 1, i.e. a selection block determines which channel is the first of being not saturated, but it also introduces a digital hystereris. The section logic follows the rising input signal, but when the input signal starts decreasing, it maintain as active the ADC channel which was last selected as appropriate for 5 clock cycles. This allows a full digitization cycle to take place through a single ADC channel, thus avoiding inter-channel calibration problems for signals spanning different scales. After 5 clock cycles the AD41240 restarts selecting its output as usual, i.e. it takes the first non-saturated of the four channels.

In this mode the output bus is 14 bit wide and outputs data at 40 MHz.

Mode 4 behaves as mode 2 but it multiplexes the bus to 7 bits at 80 MHz (double data rate).

AD41240 Application Examples

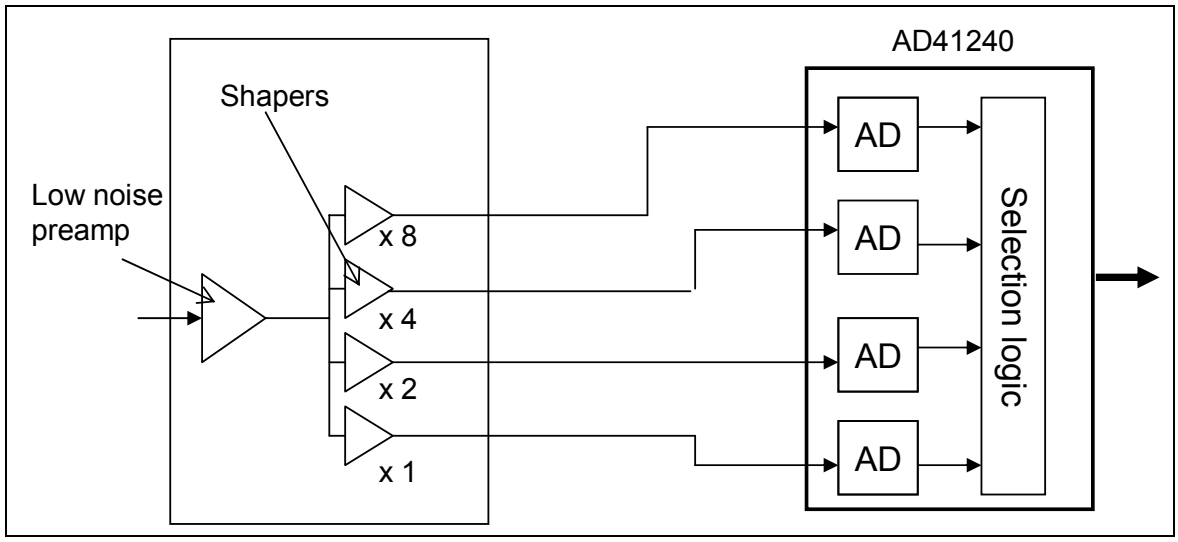


Figure 1 Large dynamic range application of AD41240

AD41240 Specifications, (specified for one channel, with device measured in operating mode 5 or 6)

Parameter	Min	Typ	Max	Units
RESOLUTION		12		Bits
DC ACCURACY				
Integral Nonlinearity				LSB
Differential Nonlinearity				LSB
Missing code				
Offset Error				%FSR
Gain Error				%FSR
ANALOG INPUT				
Input Range				V p-p
Input Capacitance				pF
DYNAMIC PERFORMANCE				
Effective number of bits				
f_{in} = 1 MHz				Bits
f_{in} = 9.9 MHz				Bits
Signal to Noise and Distortions Ratio				
f_{in} = 1 MHz				dB
f_{in} = 9.9 MHz				dB
Total Harmonic Distortions				
f_{in} = 1 MHz				dB
f_{in} = 9.9 MHz				dB
Spurious Free Dynamic Range				dB
Full Power Bandwidth				MHz
POWER SUPPLY				
Operating Voltage				
AV_{DD}	2.25	2.5	2.625	Volts
DV_{DD}	2.25	2.5	2.625	Volts
Operating Current				
IAV_{DD}				mA
IDV_{DD}				mA
POWER CONSUMPTION		450		mW
TEMPERATURE RANGE	-10	20	70	ºC

Timing Specifications, (specified for one channel, with device measured in operating mode 5 or 6)

Parameter	**Min**	**Typ**	**Max**	**Units**
Maximum conversion rate		12		Bits
Clock Period				
Clock High				LSB
Clock Low				LSB
Output delay				
Pipeline Latency				%FSR
Aperture Delay				%FSR
Aperture Jitter				

Pin Function Description

Pin Name	fpBGA144 Matrix No.	PGA120 pin	Function	Type
GNDA	pp2a		Analog GND	Power
GNDA	pp2a		Analog GND	Power
VinA1-	A1	C3	Negative input ch 1	Analog IO
VinA1+	B1	B2	Positive input ch 1	Analog IO
VDDA	pp1a	B1	Analog VDD	Power
GNDA	pp2a	D3	Analog GND	Power
VrefA1-	C1	C2	Ref Voltage	Analog In
VrefA1+	C2	C1	Ref Voltage	Analog In
VDDA	pp1a	D2	Analog VDD	Power
GNDA	pp2a	E3	Analog GND	Power
VrefA2+	E3	D1	Ref Voltage	Analog IO
VrefA2-	E4	E2	Ref Voltage	Analog IO
VDDA	pp1a	E1	Analog VDD	Power
GNDA	pp2a	F3	Analog GND	Power
VinA2+	E1	F2	Positive input ch 2	Analog In
VinA2-	E2	F1	Negative input ch 2	Analog In
VDDA	pp1a	G2	Analog VDD	Power
GNDA	pp2a	G3	Analog GND	Power
GNDA	pp2a		Analog GND	Power
VDDA	pp1a		Analog VDD	Power
VinB1-	H1	G1	Negative input ch 3	Analog In
VinB1+	H2	H1	Positive input ch 3	Analog In
VDDA	pp1a	H2	Analog VDD	Power
GNDA	pp2a	H3	Analog GND	Power
VrefB1-	H3	J1	Ref Voltage	Analog IO
VrefB1+	H4	J2	Ref Voltage	Analog IO
VDDA	pp1a	K1	Analog VDD	Power
GNDA	pp2a	J3	Analog GND	Power
VrefB2+	L1	K2	Ref Voltage	Analog IO
VrefB2-	M1	L1	Ref Voltage	Analog IO
VDDA	pp1a	M1	Analog VDD	Power
GNDA	pp2a	K3	Analog GND	Power
VinB2+	K1	L2	Positive input ch 4	Analog In
VinB2-	K2	N1	Negative input ch 4	Analog In
VDDA	pp1a		Analog VDD	Power
VDDA	pp1a		Analog VDD	Power
Ibext	L2	L3	Reference Current Monitor	Analog IO
EnClkReg	K3	M2	Enable Clk to Reg	Digital In (CMOS)
ClkReg+	K5	N2	Clk Register	Digital In (LVDS)
ClrReg-	K6	L4	Clk Register	Digital In (LVDS)
Error	L3	M3	Error Flag	Digital Out(CMOS)
Mode2	M2	N3	Mode Configuration bit 2	Digital In (CMOS)
Mode1	M3	M4	Mode Configuration bit 1	Digital In (CMOS)
Mode0	K4	L5	Mode Configuration bit 0	Digital In (CMOS)
GND	pp2b			Power
CLKIN+	M4	N4	LVDS clkin +	Digital In (LVDS)
CLKIN-	L4	M5	LVDS clkin -	Digital In (LVDS)
GND	pp2b	N5		Power
GND	pp2b			Power
VDD	pp1b	L6		Power
DoutB11-	L5	M6	Data Out Bit11- (ch 3-4)	Digital Output (LVDS)

DoutB11+	M5	N6	Data Out Bit11+	Digital Output (LVDS)
DoutB10-	L6	M7		Digital Output (LVDS)
DoutB10+	M6	L7		Digital Output (LVDS)
DoutB9-	L7	N7		Digital Output (LVDS)
DoutB9+	M7	N8		Digital Output (LVDS)
DoutB8-	L8	M8		Digital Output (LVDS)
DoutB8+	M8	L8		Digital Output (LVDS)
GND	pp2b	N9		Power
VDD	pp1b	M9	Positive digital supply	Power
DoutB7-	L9	N10		Digital Output (LVDS)
DoutB7+	M9	L9		Digital Output (LVDS)
DoutB6-	L10	M10		Digital Output (LVDS)
DoutB6+	M10	N11		Digital Output (LVDS)
GND	pp2b	N12		Power
VDD	pp1b	L10		Power
VDD	pp1b			Power
VDD	pp1b			Power
CLKOUTB+	M11	M11	Output LVDS clk+	Digital Output (LVDS)
CLKOUTB-	M12	N13	Output LVDS clk-	Digital Output (LVDS)
GND	pp2b			Power
VDD	pp1b			Power
DoutB5-	J10	L11		Digital Output (LVDS)
DoutB5+	K10	M12		Digital Output (LVDS)
DoutB4-	L11	M13		Digital Output (LVDS)
DoutB4+	L12	K11		Digital Output (LVDS)
GND	pp2b	L12		Power
VDD	pp1b	L13		Power
DoutB3-	K11	K12		Digital Output (LVDS)
DoutB3+	K12	J11		Digital Output (LVDS)
DoutB2-	J11	K13		Digital Output (LVDS)
DoutB2+	J12	J12		Digital Output (LVDS)
GND	pp2b			Power
VDD	pp1b			Power
DoutB1-	H11	J13		Digital Output (LVDS)
DoutB1+	H12	H11		Digital Output (LVDS)
DoutB0-	G11	H12	Data Out Bit0-	Digital Output (LVDS)
DoutB0+	G12	H13	Data Out Bit0+ (ch 3-4)	Digital Output (LVDS)
GND	pp2b	G12		Power
VDD	pp1b	G11		Power
DoutA11-	F11	G13	Data Out Bit11- (ch 1-2)	Digital Output (LVDS)
DoutA11+	F12	F13	Data Out Bit11+	Digital Output (LVDS)
DoutA10-	E11	F12		Digital Output (LVDS)
DoutA10+	E12	F11		Digital Output (LVDS)
GND	pp2b			Power
VDD	pp1b			Power
DoutA9-	D11	E13		Digital Output (LVDS)
DoutA9+	D12	E12		Digital Output (LVDS)
DoutA8-	C11	D13		Digital Output (LVDS)
DoutA8+	C12	E11		Digital Output (LVDS)
GND	pp2b	D12		Power
VDD	pp1b	C13		Power
DoutA7-	B11	B13		Digital Output (LVDS)
DoutA7+	B12	D11		Digital Output (LVDS)
DoutA6-	D10	C12		Digital Output (LVDS)
DoutA6+	C10	A13		Digital Output (LVDS)
GND	pp2b			Power

VDD	pp1b			Power
GND	pp2b	C11		Power
VDD	pp1b	B12		Power
CLKOUTA-	A12	A12	Output LVDS clk-	Digital Output (LVDS)
CLKOUTA+	A11	C10	Output LVDS clk+	Digital Output (LVDS)
DoutA5-	B10	B11		Digital Output (LVDS)
DoutA5+	A10	A11		Digital Output (LVDS)
DoutA4-	B9	B10		Digital Output (LVDS)
DoutA4+	A9	C9		Digital Output (LVDS)
GND	pp2b	A10		Power
VDD	pp1b	B9		Power
DoutA3-	B8	A9		Digital Output (LVDS)
DoutA3+	A8	C8		Digital Output (LVDS)
DoutA2-	B7	B8		Digital Output (LVDS)
DoutA2+	A7	A8		Digital Output (LVDS)
GND	pp2b			Power
VDD	pp1b			Power
DoutA1-	B6	B7		Digital Output (LVDS)
DoutA1+	A6	C7		Digital Output (LVDS)
DoutA0-	B5	A7	Data Out Bit0-	Digital Output (LVDS)
DoutA0+	A5	A6	Data Out Bit0+ (ch 1-2)	Digital Output (LVDS)
GND	pp2b			Power
GND	pp2b	B6		Power
VDD	pp1b			Power
VDD	pp1b	C6		Power
enadc1	A4	A5	Enable adc 1	Digital In (CMOS)
anadc2	C4	B5	Enable adc 2	Digital In (CMOS)
enadc3	B4	A4	Enable adc 3	Digital In (CMOS)
enadc4	B3	C5	Enable adc 4	Digital In (CMOS)
GNDA	pp2a		Analog GND	Power
GNDA	pp2a	B4	Analog GND	Power
GNDA	pp2a		Analog GND	Power
VDDA	pp1a		Analog VDD	Power
VDDA	pp1a	A3	Analog VDD	Power
VDDA	pp1a		Analog VDD	Power
Vcm	A3	A2	Common Mode Voltage	Analog Out
Vbg	A2	A1	Bandgap reference voltage	Analog IO

Outline dimensions