Kchip: A Radiation Tolerant Digital Data Concentrator chip for the CMS Preshower Detector

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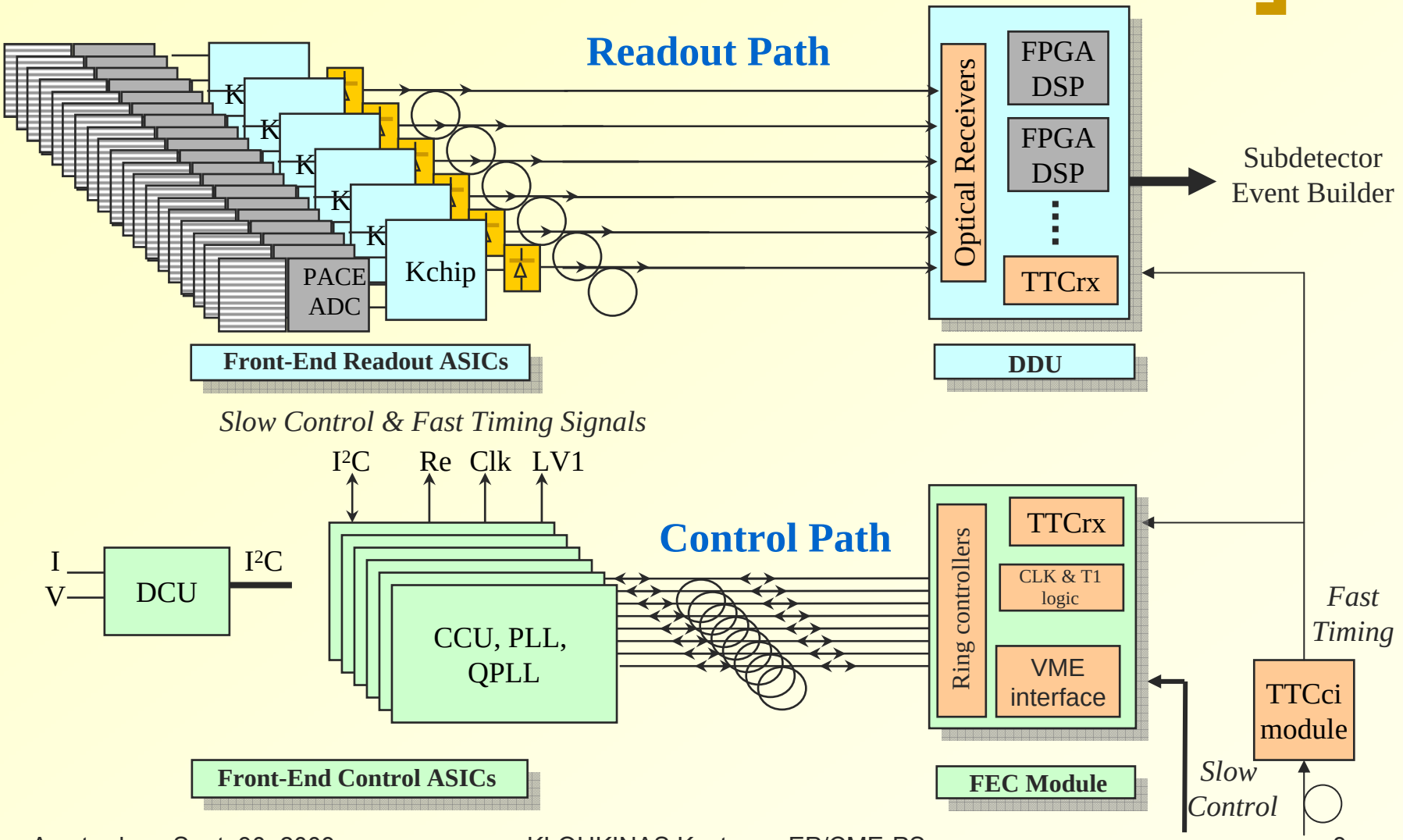
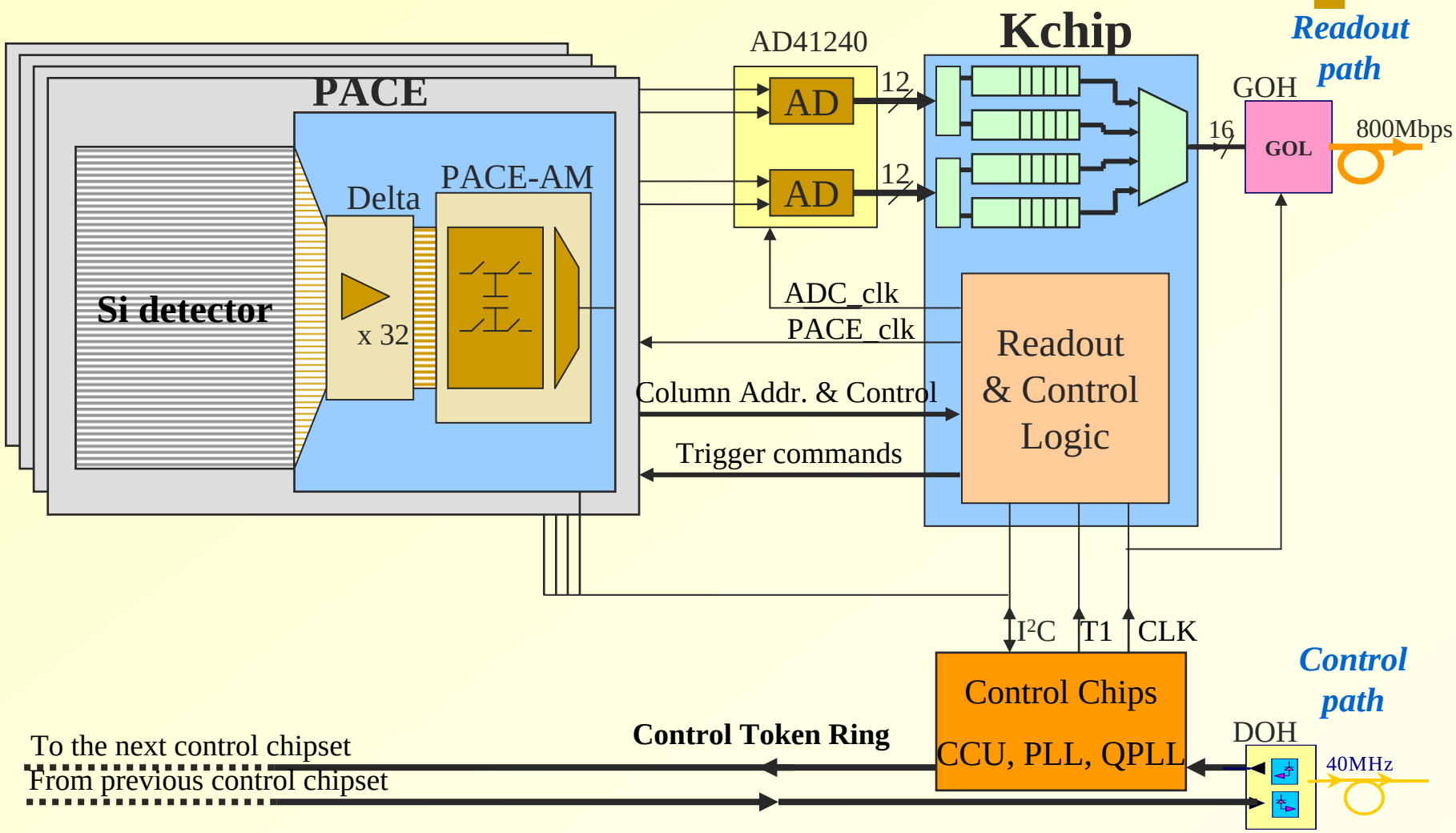
Outline

- Preshower Front-End System
- Kchip Architecture
- Kchip Implementation
- Prototype Test Results

Preshower Front-End System



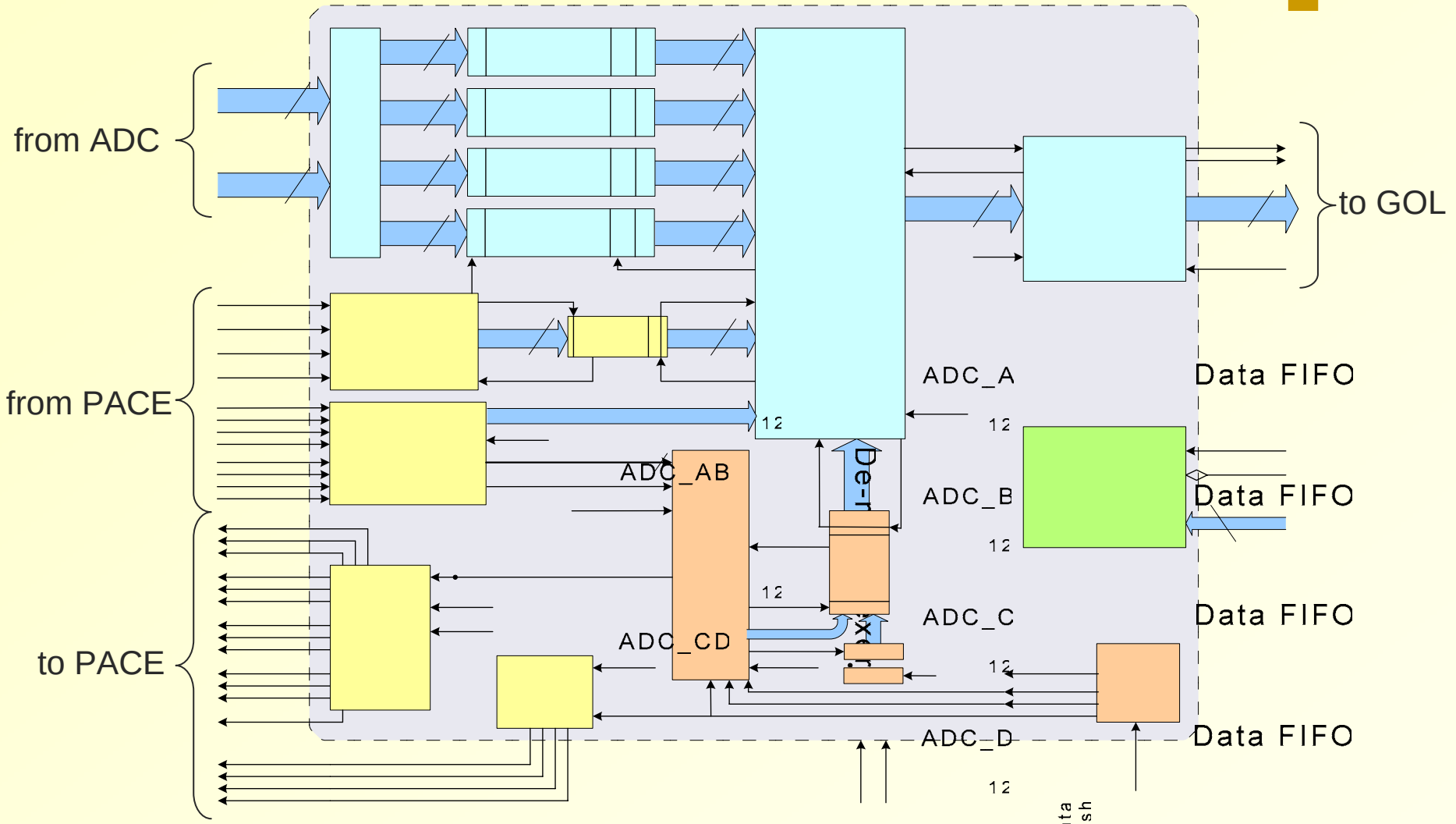
Preshower Front-End Readout



Kchip Functionality

- Data Concentration
  - Can be configured to readout 1~4 PACE chips.
- Event Data Formatting
  - Align data into 16-bit words.
  - Assemble an Event Packet.
  - Assign a Bunch Count (BC) and Event Count (EC) Identifier.
  - Link Protocol for transmission through a Gigabit Optical Link.
- Readout Controller
  - Trigger Command Decoding
  - PACE Readout Synchronization Monitoring
  - Front-End Buffers Overflow Detection / Prevention
  - PACE & ADC clock and Trigger Command Distribution

Kchip Block Diagram

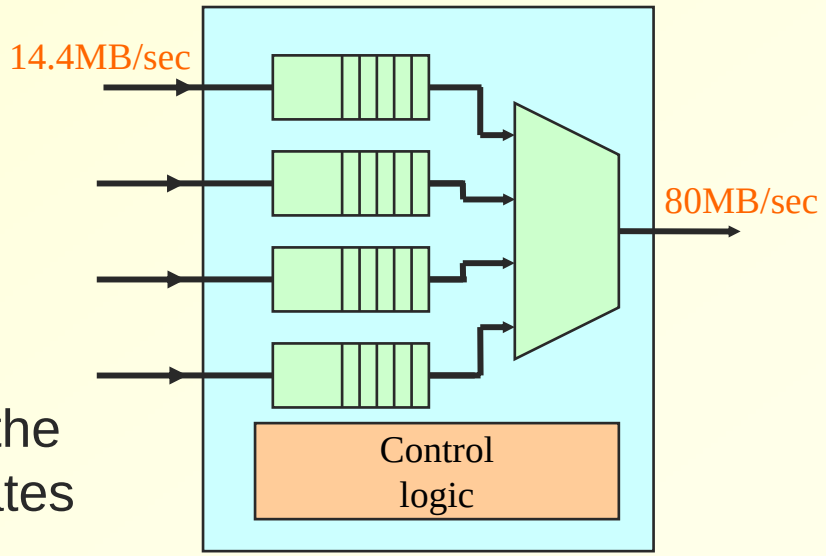


Data Rates

- PACE generated traffic

3 columns/trigger
32 samples/column
} 96 samples/trigger
12-bit ADC
100KHz Trigger Rate
} 14.4 MB/sec

Traffic from 4 PACE chips = 57.6MB/sec



- Gigabit Link Throughput

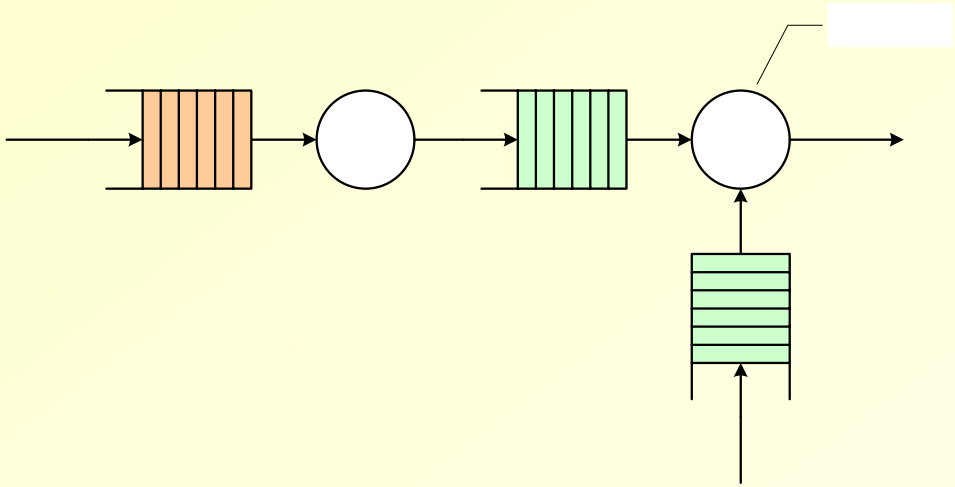
(GOL chip) 80 MB/sec

PACE event readout time = 6.9 µsec
Kchip event readout time = 7.8 µsec

- The difference in the readout times and the stochastic nature of trigger arrivals mandates the need of data buffering on the Kchip.

Front-End System FIFOs

- Model of front-end system FIFOs.



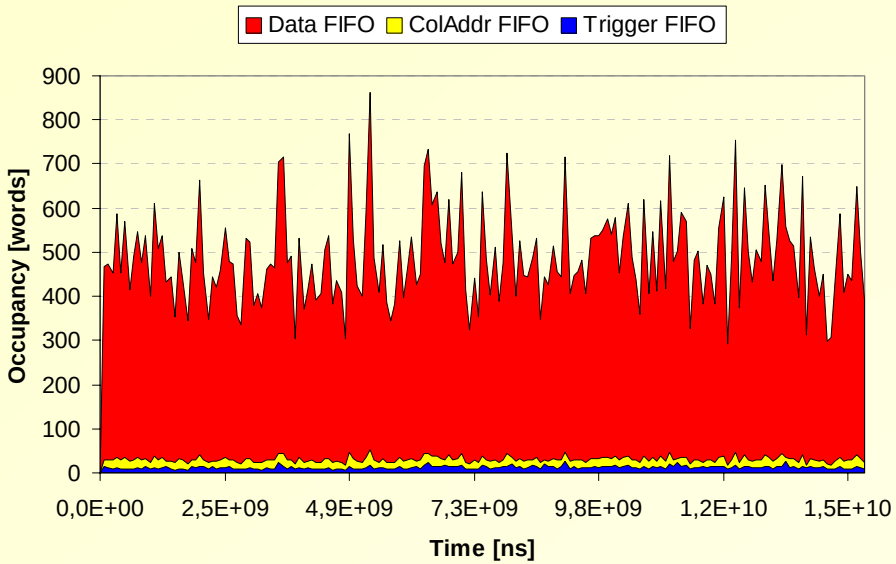
- Trigger arrivals follow an exponential distribution.
- Kchip service time follow a uniform distribution. PACE FIFO
  - An analytic queuing model is difficult to develop.
  - A simulation model of the complete front-end system has been developed.

λ_{LV1}

μ_P

Sizing the Kchip FIFOs

- PACE FIFO can store up to 10 events.
  - From simulations: $P_{rejection}$= 1.9E-04 @ 100KHz trigger rate.
- Kchip FIFOs:
  - Kchip FIFOs should be sized for lower event rejection probability.

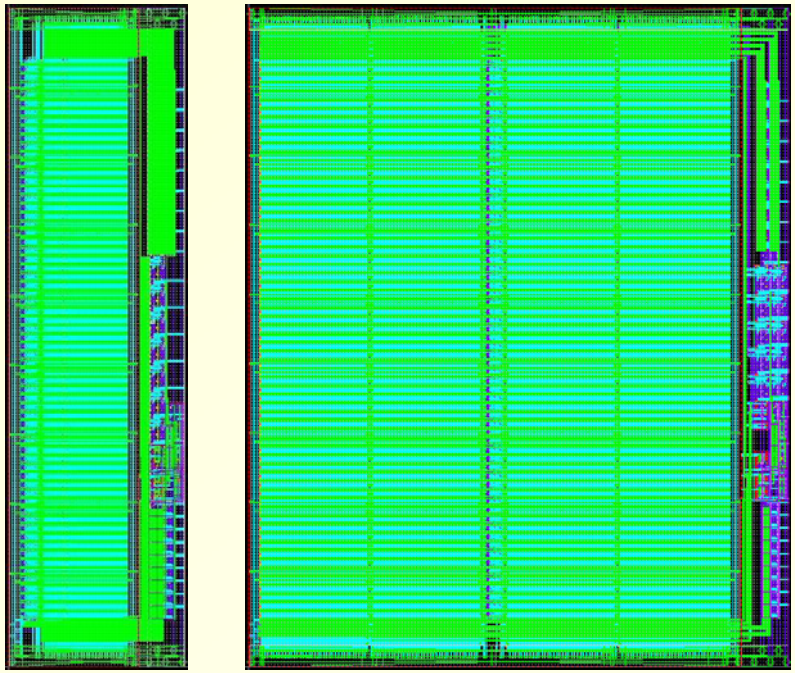


Time examined	15.10^2	s
Number of events	$1.5\ 10^6$	
Mean interarrival time of events	10.059	µs
PACE rejected events	7	
Kchip rejected events	0	
Maximum Trigger FIFO occupancy	26	words
Maximum Column FIFO occupancy	52	words
Maximum Data FIFO occupancy	863	words
Average Trigger FIFO occupancy	3	words
Average Column FIFO occupancy	2	words
Average Data FIFO occupancy	36	words

Implementation of Kchip FIFOs

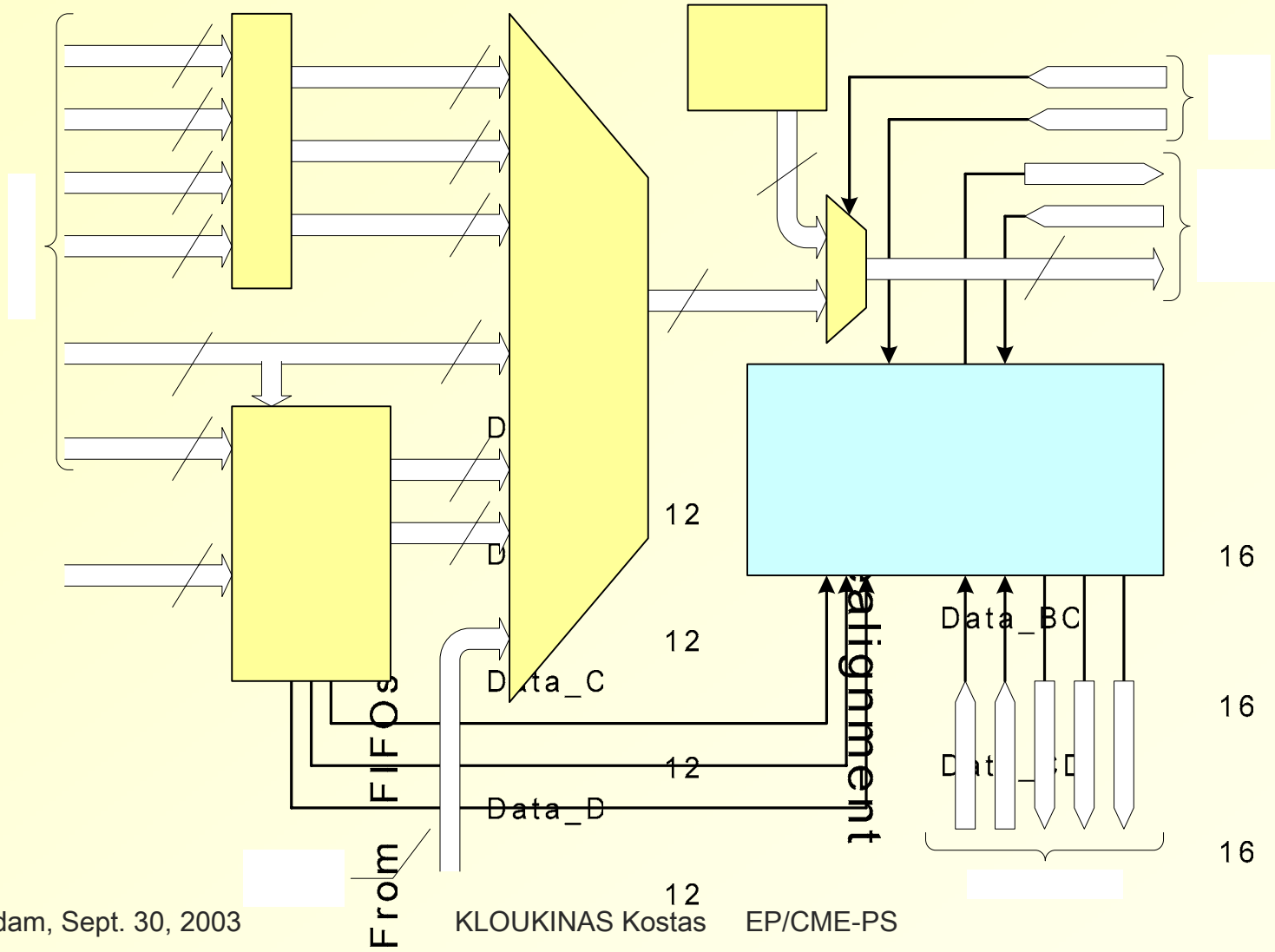
FIFO	Native Size of SRAM module	Actual Capacity
Data	1 Kword x 18 bits	10 events (1024/96)
Column Address	128 words x 27 bits	10 events (matches Data FIFO)
Trigger	128 words x 27 bits	64 triggers (128/2)

- FIFOs are implemented using a "Configurable Dual-Ported SRAM macro cell".
- Two macro cells:
  - Column Addr. & Trigger FIFO
    - 128 words x 27 bits
  - Data FIFO
    - 1024 words x 18 bits

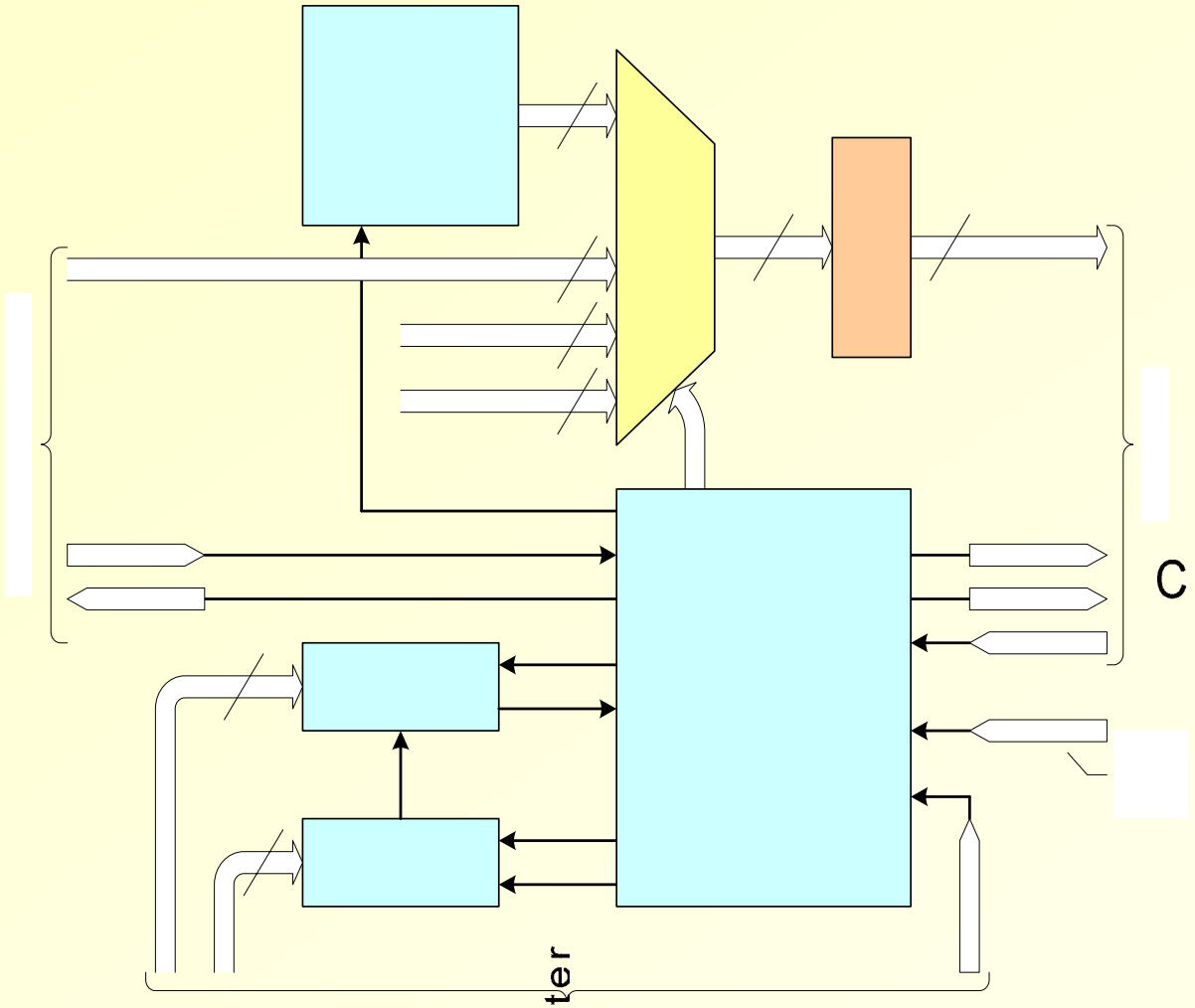


128 x 27bits 1024 x 18bits

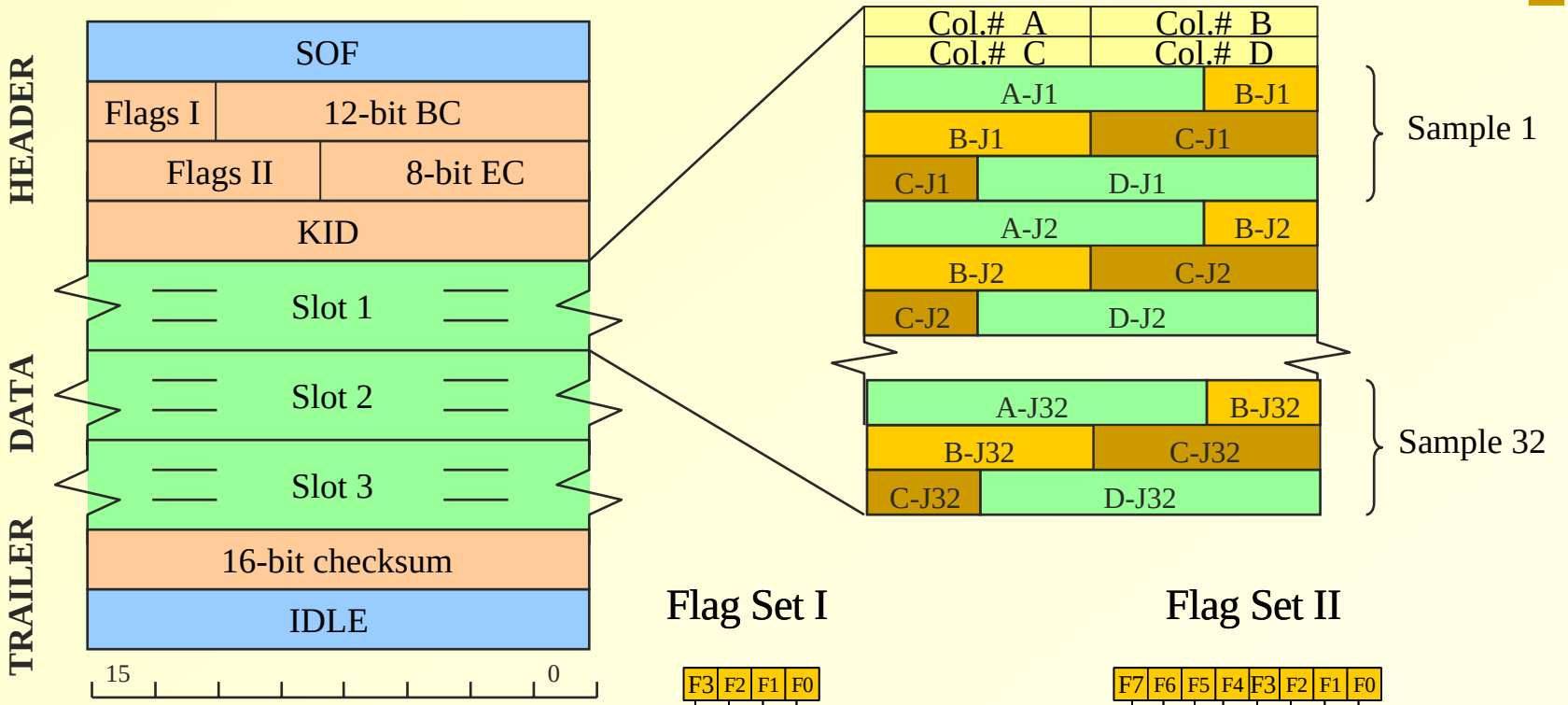
Packet Formatter

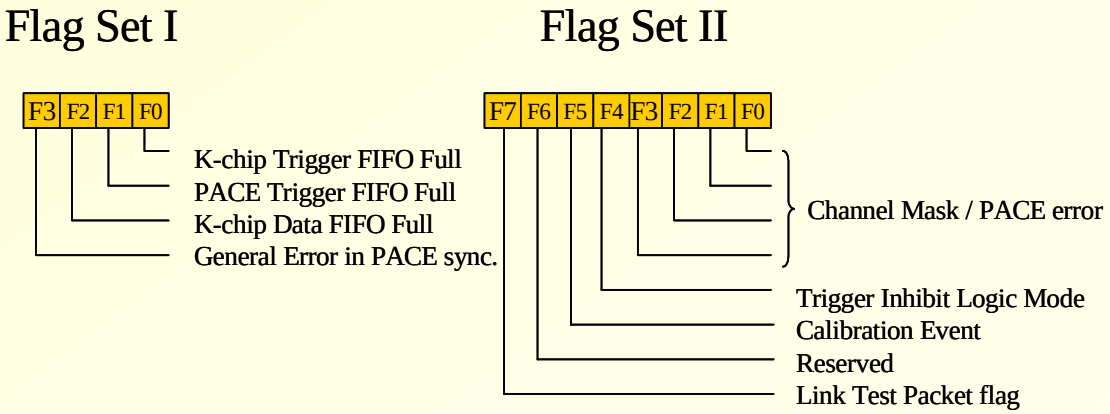


GOL Interface



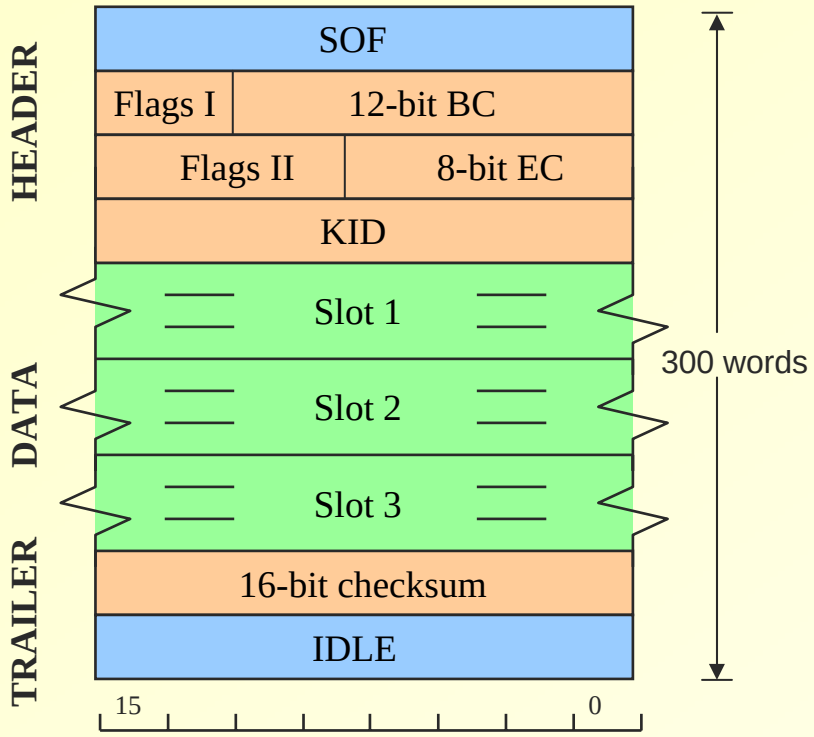
Packet Format



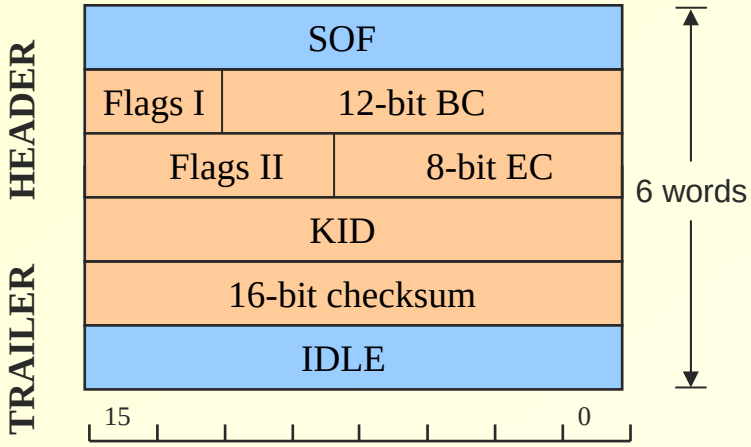


Packet Types

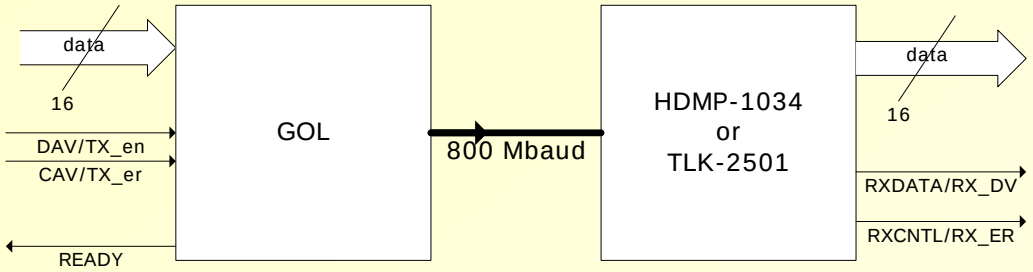
Normal Event



Null Event



Link Layer

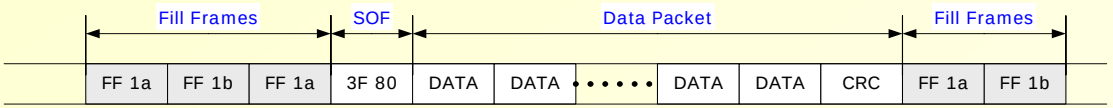


- The Kchip employs a packet oriented data transmission protocol.
- The Kchip Link Layer Protocol uses two uniquely defined transmission control characters, the IDLE and the SOH.
  - The IDLE character allows the receiver to obtain and maintain bit synchronization. .
  - The SOF character indicates the beginning of the frame and delimits the boundaries of subsequently transmitted frames.

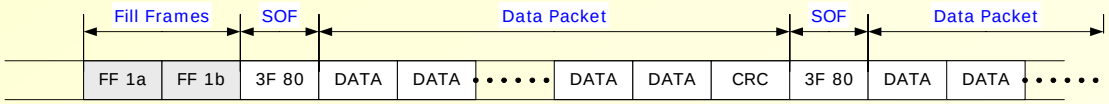
Link Protocol

- The Kchip can seamlessly use both encoding schemes supported by the GOL chip: the CIMT and the 8b/10b encoding.
  - The flexibility of using both encoding schemes is realized by properly choosing transmission control symbols (SOF, IDLE) which are supported in both encoding schemes.

CIMT encoding

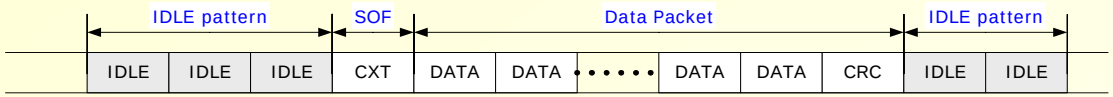


Packet format in CIMT encoding.

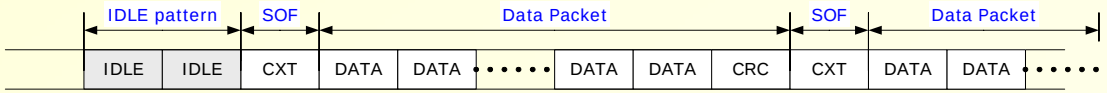


Packet format in CIMT encoding for back-to-back events.

8b/10b encoding



Packet format in 8b/10b encoding.



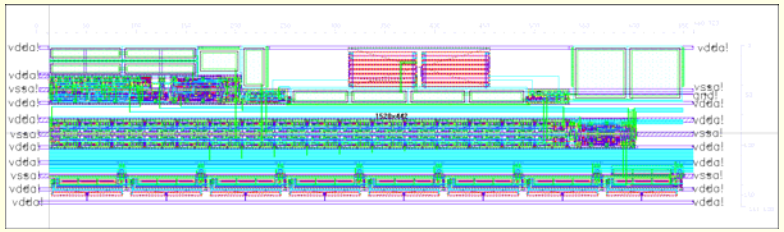
IDLE = <K28.5, D5.6> or <K28.5, D16.2> : Idle
CXT = <K23.7, K23.7> : Carrier Extend

Packet format in 8b/10b encoding for back-to-back events.

Calibration Circuit & DLL

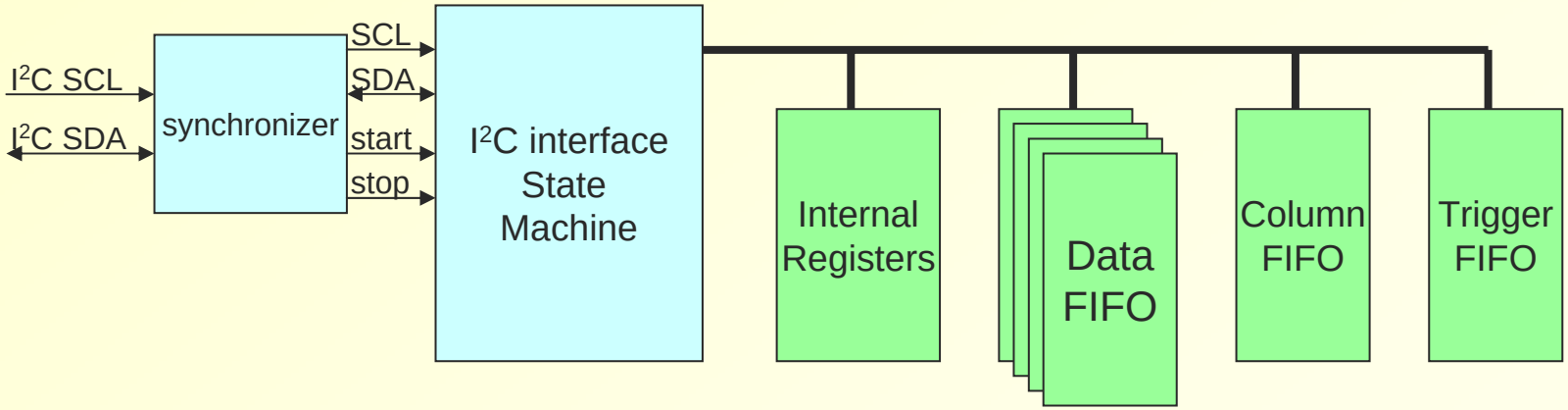
- The Kchip distributes to the PACE chips a calibration pulse of programmable delay with respect to the system clock and with programmable width (1 – 256 cycles).
- The DLL from APV25 chip has been ported into the Kchip.
  - Delay adjustment: 16 steps of 3.25ns
- After an interval equal to the trigger latency a Trigger signal is generated by the Kchip in order to readout the Calibration Data.
  - The automatic generation of the Calibration Event can be disabled.

The DLL block as delivered from RAL.



I²C Interface

- The I²C interface can be used to access:
  - The Kchip Internal Registers (There are 25 Status & Control Registers).
  - The Kchip FIFOS (Data, Column Addr. and Trigger FIFOs).
- Supports 7-bit addressing Single Byte transfers.
- Synchronous design. (40MHz system clock)



Buffer Overflow Handling

- The Kchip can detect imminent overflow conditions and prevent buffers from actually overflowing and lose synchronization.

- Trigger Inhibit Logic on Kchip.
  - If a FIFO signals an *Almost Full* condition then the Trigger signal will be gated until some data has been read out and space is made available.
  - The readout chain gets informed about the trigger gating condition and NULL Events are inserted to maintain Event Readout Synchronization.
  - The Trigger Inhibit logic can be enabled or disabled.

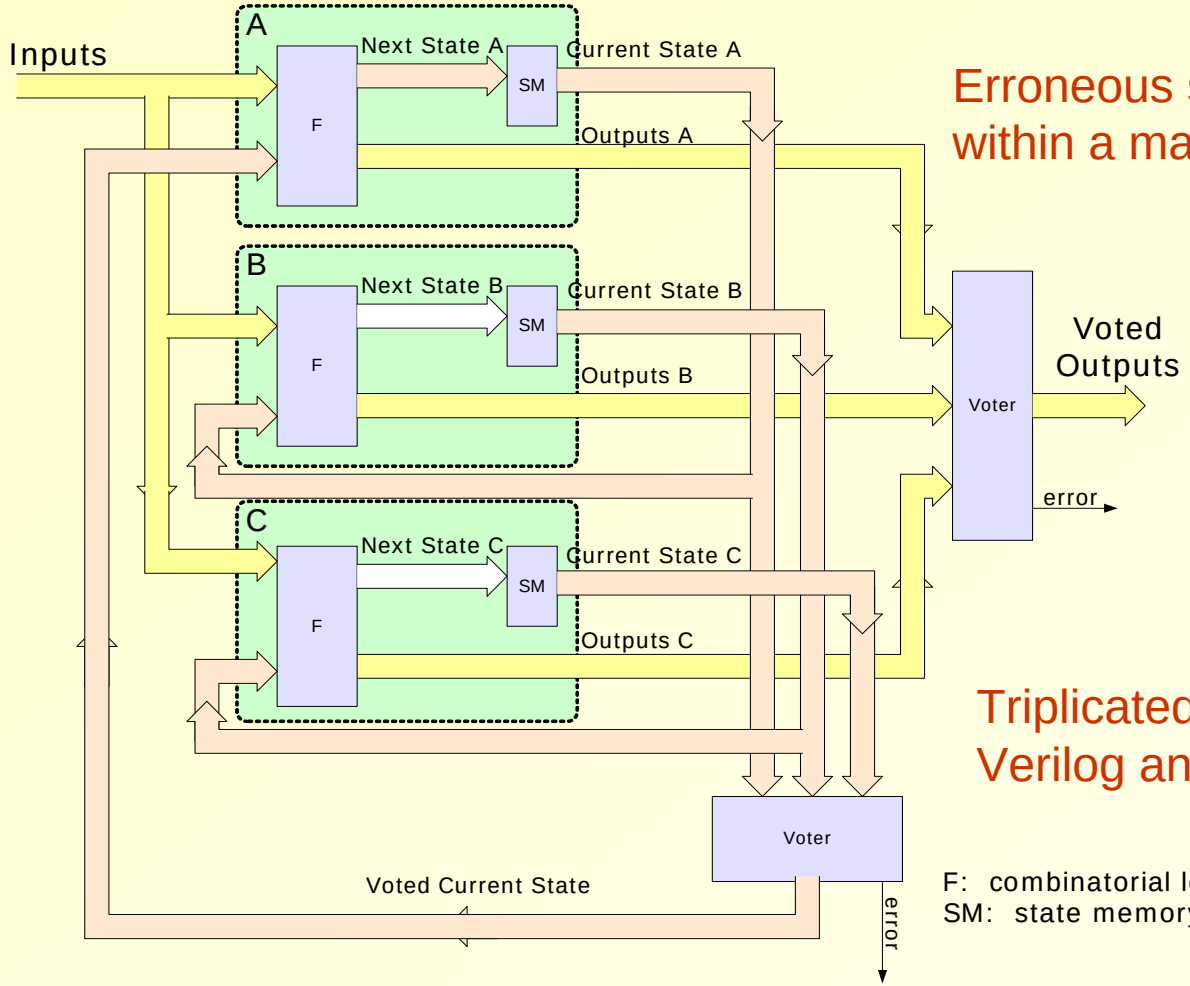
PACE synchronicity monitoring

- Under normal operation the pipeline memories in the PACE chips should run synchronously.
- The Kchip monitors the synchronization of the PACE chips by comparing the status of their control signals on a cycle to cycle basis.
  - Cross-checks the 4 “DataValid” signals.
  - Cross-checks the 4 “AlmostFull” signals.
- “PACE out of sync” condition is signaled when the readout sequence in any of the PACE chips is not synchronous to the Kchip internal readout sequencer.
- The “PACE out of sync” condition is flagged in the data packet header and in a special status register accessible through the I^2C bus.

Implementation Issues

- SEU Tolerant Design
  - Protect Control Logic using Triple Module Redundancy.
    - All State Machines and Configuration Registers have been triplicated.
  - Leave Data Path unprotected.
    - SEU errors affect the integrity of small amount of information and does not lead to a loss of readout synchronization.

Triplicated State Machine

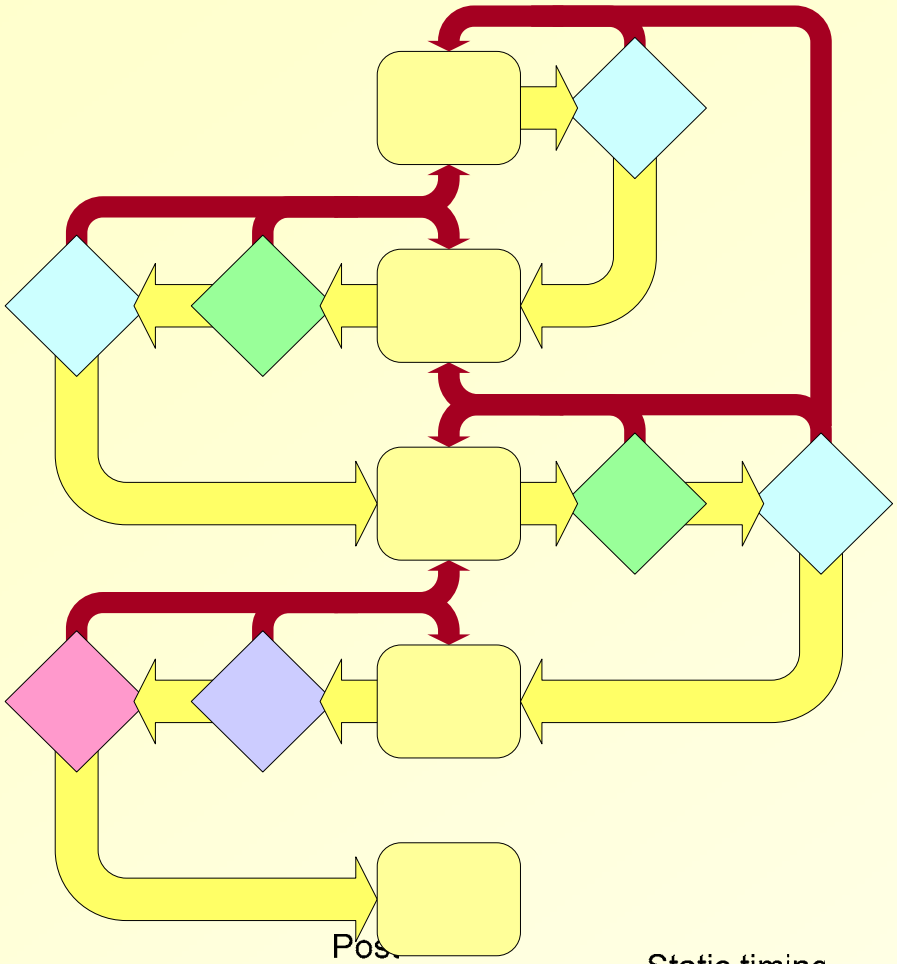


Erroneous state machine will recover within a maximum of 3 clock cycles.

Triplicated logic was described in Verilog and has been synthesized.

F: combinatorial logic
SM: state memory

Kchip Design flow



- Design implemented using the CERN DSM Design Kit in 0.25μm commercial CMOS technology.

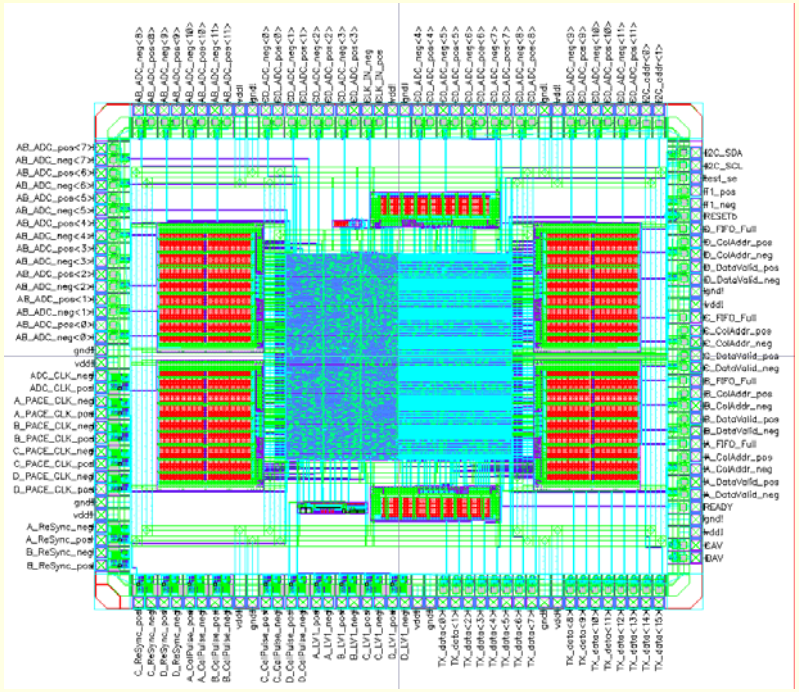
- Hardware Description Language: Verilog
- Automatic synthesis and layout: Synopsys, Silicon Ensemble
- Verilog XL simulation
- Static timing analysis: Pearl
- Design flow is “scripted”.

- Design for Testability
  - I^2C port
    - can be used to access and test the on-chip SRAMs
  - Scan Path
    - For design debugging and production testing.

The Synthesized Chip

- Number of Digital Standard cells
  - Registers: 1,400
  - Gates: 13,300
- Clock tree statistics
  - Number of buffers: 189
  - Number of Levels: 6
  - Max. delay: 685 ns
  - Max. skew: 65 ps
- Special Macro Cells
  - 4x 1024 x 18bit, dual-port SRAM
  - 2x 128 x 27bit, dual-port SRAM
  - DLL
- Number of pad cells
  - I/O pins: 131
  - Power pins: 17
  - Total pins: 148

Size: 6 x 5 mm²
Pad Limited design.



Kchip Layout

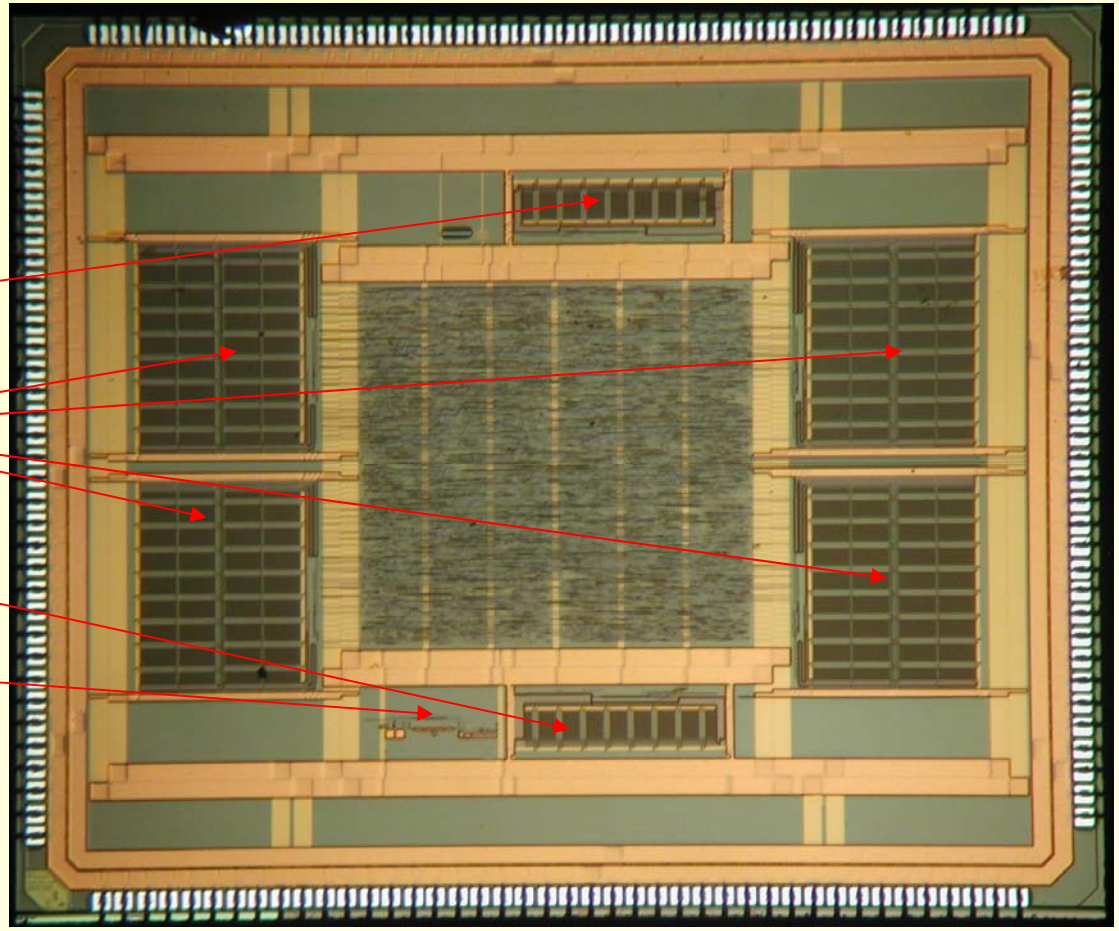
1st Prototype
CERN MPW10
Submitted: Feb. 2003
Received: June 2003

Column Addr. FIFO

Data FIFOs

Trigger FIFO

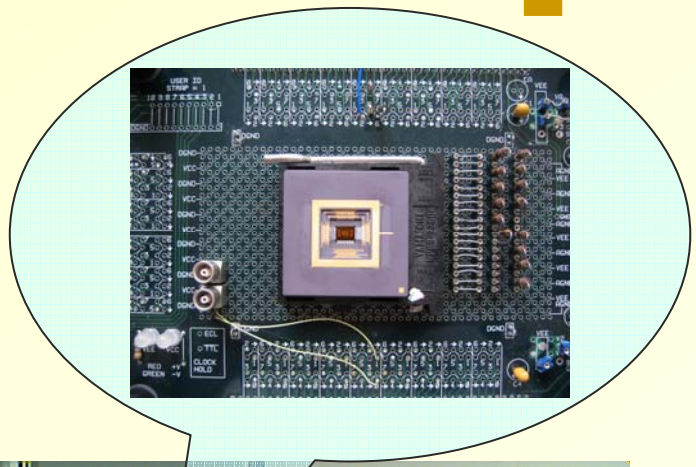
DLL block

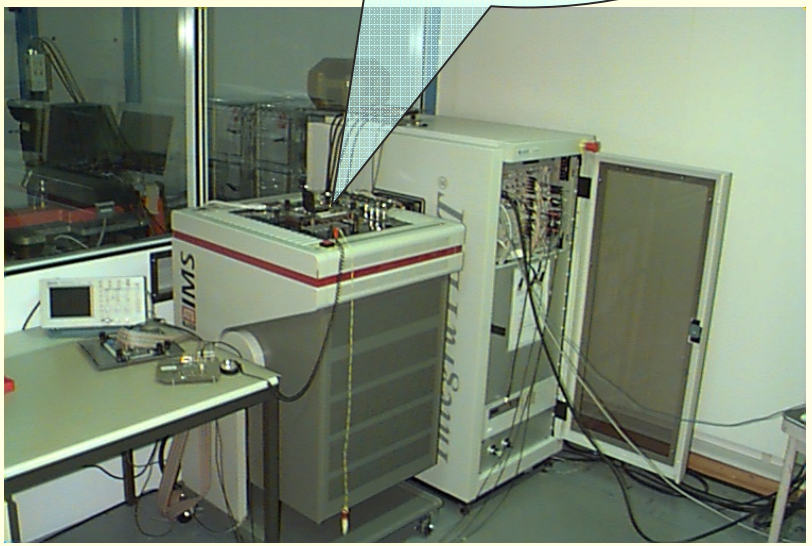


Kchip designers:
Kostas Kloukinas, CERN EP/CME
Sandro Bonacini, CERN EP/MIC

Prototype Tests

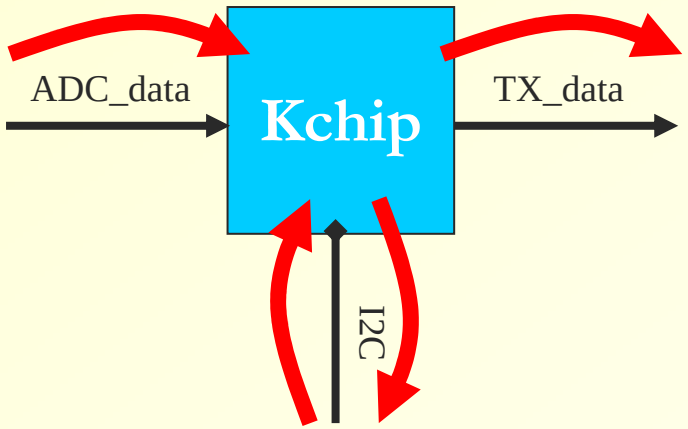
- Scope
  - Test functionality & validate specifications conformity.
- Method
  - Make use of a Digital Tester at CERN (MIC group).
  - Use a generic “Test Fixture” board to host the chip.
  - Use a ceramic package (CPGA) to facilitate bonding.
  - “Test Vectors” were generated from Front-End system simulations.





Test Pattern sequences

- (a) Kchip in Test Mode
  - Access on-chip FIFOs and internal registers through the I^2C interface.
- (b) Kchip in Test Mode
  - Filling the on-chip FIFOs from the ADC bus and then reading data back through the I^2C interface.
- (c) Kchip in Test Mode
  - Loading data into the FIFOs through the I^2C interface and then reading it out from the GOL bus.
- (d) Kchip in Normal Mode
  - Sending triggers and reading out events through the GOL.



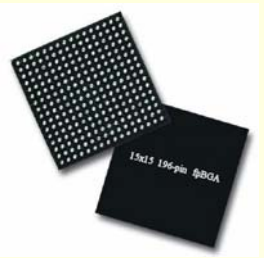
Prototype Test Results

- The functionality of the Kchip has been successfully verified.
  - Various data traffic patterns were simulated and test vectors were loaded to the tester for verification.
    - All modes of operation have been verified.
    - No loss of readout synchronization up to 200KHz trigger rate (Poisson distribution).
  - I^2C Interface
    - I^2C interface maximum speed: 3.33 Mbit/s.
    - Kchip has been tested with the CCU chip.
  - All Internal Registers were accessible. ID fuse bits were read out.
  - Calibration Event Generation Logic
    - Verified the Programmable Timing of the CalPulse (on chip DLL)
- A layout bug in the Data FIFO SRAM module has been identified.
  - In specific traffic conditions, some data packets (0.5%) had errors in the data field.

Prototype Test Results

- Maximum operating frequency: 60MHz
  - The limiting factor was due to the bug in the SRAM module.
- Power consumption
  - Test Conditions: 40MHz, VDD=2.5V, T=25^{O}C
  - I_{core} = 68mA, P_{core} = 170mW
  - I_{peri} = 182mA, P_{peri} = 455mW
  - I_{total} = 250mA, P_{total} = 625 mW
- Irradiation Tests
  - Use of an X-ray machine at CERN.
  - Step Irradiation at 1, 3, 5, 10, 20 MRad (SiO_2).
  - Dose Rate = 2.04 MRad/h
    - Devices were operational up to 20 MRad @ 2.5V, 40MHz.
    - Observed a *small drop in power dissipation*.
      - ΔI = 2% @ 10MRad.

Conclusions



- Conclusions
  - The first prototype of the Kchip has been successfully fabricated.
  - Functionality has been verified on a digital tester.
- Future Plans
  - In system tests are under preparation.
  - SEU tests will follow.
  - Submission in next MPW.
    - Implement the fix for the bug in the SRAM module.
    - Implement Hamming encoding in the FIFOs.
    - Implement Built In Shelf Test circuit for the FIFOs.
- Acknowledgements
  - Microelectronics group in Rutherford Appleton Lab. particularly Quentin Morrisey for the APV25 chip DLL macro cell.