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CMS PRESHOWER FRONT-END READOUT & CONTROL SYSTEM

DRAFT

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Notes: This document is a draft for people working on the CMS Preshower Readout and control System and serves as preliminary specifications for the system.
Please check regularly for updates.

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Document History

- **Version 0.1 DRAFT**: this is the first draft of the Preshower Front-End electronics for the readout and control system. The aim of this version of the document is to provide a baseline for the system design architecture and implementation. It should be considered as the skeleton of a specifications document where many design issues are addressed but not all are specified. At this stage of the document preparation the information presented is not validated by the people working in the system design and integration and should not be used as a basis for any development work without prior consulting the author.

1 Introduction

This document describes the architecture and a proposed implementation for the Front-end part of the Read-Out and Control system of the CMS Preshower detector. The scope of this document is only to maintain a working reference for everybody contributing to the construction of different parts of the system. Therefore it should not be considered as a user's manual.

It covers the following topics:

- a general introduction to the Preshower front-end electronics
- the functional requirements for the read-out system
- the performance requirements
- the global timing signals and the interface to the trigger supervisor system and data acquisition system
- the proposed architecture and implementation for the digital read-out
- the slow control and timing distribution architecture for the Preshower
- power and packaging requirements
- documents describing the detailed elements and ASICs in the system are available separately.

It does not cover:

- design issues concerning the Readout System beyond the DDU (*Detector Dependent Unit*)
- design issues concerning the integration of the Preshower Control system to the overall CMS slow control system
- details about the various ASIC components used in the system.

2 Overview of the Readout & Control Architecture

2.1 Overview

The number of detectors to be read out by the Preshower electronics is 4288 for the endcap. Each detector has 32 channels; the total number of channels is therefore 137,216 for the endcap. The length of the strips is 61 mm, corresponding to approximately 40 pF capacitance. The detector is located in the forward regions between the outer shell of the tracker and the inner layer of the ECAL detector. The readout electronics for the Preshower have to fulfill the following requirements:

The charge deposited in the strips must be measured with a $\approx 5\%$ precision to ensure that the energy correction for the loss in the Preshower converter is not limited by the electronics noise.

It is necessary to detect minimum-ionizing particles (mips) in order to intercalibrate the channels. Furthermore, a low threshold is also required for photon measurements: for example, at 20 GeV, a 1.5 mip threshold would reduce the efficiency by 3.5% in the first plane of the endcap Preshower.

The electronics must have a large dynamic range to measure the energy deposition of very high energy showers. The total charge measured after 3 X_0 absorber in the silicon detectors is on average 690 mips for a 1000 GeV electron and exceeds 1000 mips for 11.5% of the events. However, the charge is spread on several strips and over two 25 ns samples, so that a 250 mips dynamic range for a single time sampling is sufficient [HM Calorimeter TDR].

The electronics should be fast in order to minimize pileup effects and to allow a reliable bunch-crossing assignment.

The power consumption must be kept to a minimum.

Each micro-strip in the Preshower is read out by a charge sensitive amplifier followed by a shaper, The output voltage of the shaper is sampled at the beam crossing rate, and the samples are stored in the cells of an analog pipeline memory for the maximum Level-1 trigger latency of 3.2 μs. Following a Level-1 trigger, for each strip a series of samples from the pipeline are digitized and transmitted through high speed optical links to the counting room. The electronics in the counting room will merge the information arriving from different parts of the Preshower detector, perform signal conditioning and zero-suppression and eventually feed with event fragments the Preshower event builder system.

2.2 General Readout & Control Architecture

The front-end electronics is organized as an analog pipeline, where events are stored on a front end chip called PACE, followed by an on-detector analog to digital conversion stage and a non-zero-suppressed data transmission system to the counting room. A simplified block diagram of the complete chain is shown in the Figure 2.1 below.

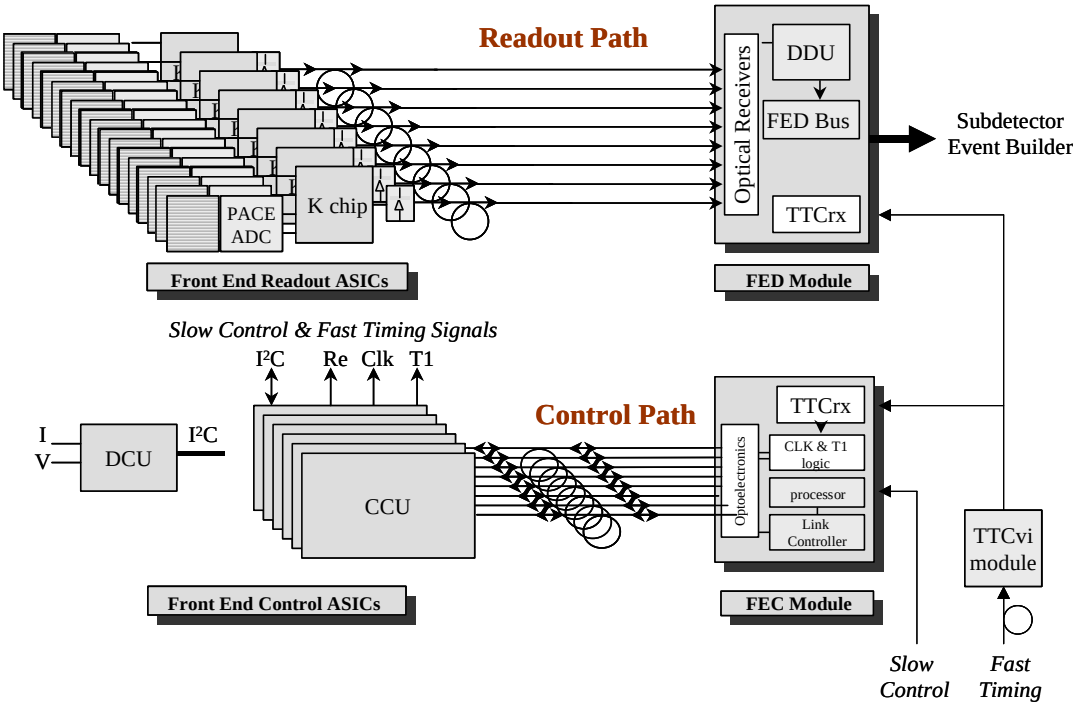


Figure 2.1 Preshower Readout & Control Architecture.

The system is composed of the following elements:

- the analog front-end ASIC chipset called PACE; their function is basically to provide an analog pipeline for the detector signals prior to digitization
- analog-to-digital converters are placed at the output of the PACE ASICs but are virtually transparent to the logic and dataflow of the read-out system
- the front-end digital K-chips collect data from a group of PACE chips and format the information in a way suitable for serial transmission
- a high speed optical link is virtually a transparent connection medium between the electronics embedded on the detector and the electronics in the counting room
- data are using the serial links into the Front-End-Driver (FED) modules, which have the function of performing some data reduction and a limited amount of event building
- a sub-detector event builder collects all pieces of data belonging to the Preshower in a fashion compatible with the general CMS DAQ system

- a trigger supervisor (*not shown in the diagram above*) might be in use to control the distribution of the trigger signals to the front-end as a function of the occupancy of the front end buffers. Essentially the trigger supervisor monitors that no trigger is sent to the front end if the front-end has reached a very high level of occupancy, due to a trigger congestion. The trigger supervisor also informs the FEDs of the arrival of normal events blocks which the FED has to assemble in sub-events before transmitting to the event builder.

- the front-end control ASICs, namely the CCU (*Communication and Control Unit*), the PLL (*Phased Locked Loop*) and the DCU (*Detector Control Unit*). The PLL-CCU pair of chips is responsible for distributing fast timing control signals to the front-end readout ASICs and provides system monitoring and control capabilities. The DCU ASIC is dedicated to local measurement of environmental parameters.

- a low speed (40MHz) bi-directional optical link is used to deliver the fast timing signals (LHC_clk, LV1, Reset, etc) to the embedded electronics and also to relay control and status information between the embedded electronics and the electronics on the counting room

- The FEC (*Front End Control*) module is situated in the counting room and handles 8 control links. Its task is to encode and transmit the fast timing signals along with some slow control commands through the control links and to receive status information from the front-end ASICs.

2.3 Readout System Requirements

2.3.1 System requirements

The Preshower electronics still receives a considerable amount of ionizing radiation (~ 3 MRad in ten years) and of neutrons (~ 10^{14} neutrons/cm^2). This rules out the utilization of commercial solutions also for the relatively straightforward digital part of the chain and custom ASICs have to be developed.

The constraints on a reliable read-out architecture are summarized briefly as follows:

- Detector signals from the silicon strips have a very large dynamic range (~12 bits) with stringent requirements on resolutions on the low end of the scale (> 8 bits). This prevents an immediate conversion of the signal to digital (would require a high speed, high resolution A/D per silicon strip) and also the utilization of an analog transmission system to the external world, as such a high dynamic range analog optical link has not yet been proven. Table 2.1 summarizes the requirements for the analog part of the Preshower Front-End electronics.

- Detector channel occupancy in the Preshower is expected to be in the 2-4% range. Despite the fact that such a low occupancy would ideally be exploited with a fast and simple data reduction system, zero-suppression on detector is not considered as "safe" by the physicists, as a fully safe and efficient filtering algorithm has not yet been demonstrated. This requires the availability of high speed data links. A similar solution was

taken in the ECAL calorimeter and the Preshower imitates that architecture in this sense.

- Transmission of data from the detector to the outside world is ideally achieved with a high speed serial, packet oriented medium. Several commercial components would exist satisfying the bandwidth required for the Preshower, but none exists with the required radiation hardness and low power characteristics within an affordable price-range.

- A general purpose slow control bus is necessary to access configuration and mode registers in the front end. In addition all ASICs need the LHC clock and some of them the trigger and other synchronization signals such as a reset. The slow control and timing distribution requirements in the Preshower are very similar to those of several other CMS sub-detectors. An architecture virtually identical to the one used in the tracker has been proposed. This is based on a bi-directional optical data link shared among the timing and slow control system. The link operates at the LHC standard 40.08 MHz and is also used for the distribution of the trigger signal. A hierarchical slow control bus based on a high-level Token-Ring like architecture followed by a local distribution system following the I2C standard is used to download and access internal ASIC configuration and status registers.

Table 2.1 Specifications for the analog electronics for Preshower detectors

Parameter	Value	Comment
Channels/chip	32	
Dummy channels/chip	4	for common noise subtraction
Sampling frequency	40 MHz	
Equivalent noise charge	2500 e – for 40 pF	(25 ns time slot) leakage current not included
Coupling	DC	
Maximum leakage current	40 mA	
Number of integrating slices	3	2 for signal, 1 for pedestal
Memory depth	4 ms	160 time slices
Gain	10 mV/mip	
Dynamic range	250 mips	12 bits
Memory non-uniformity	0.8 mV r.m.s max.	
Power consumption	10 mW/channel	ADC not included
Non-linearity	2% max.	
Radiation hardness	> 10 Mrad, 2×10^{14} n/cm 2	

2.3.2 Expected Data rates

This paragraph gives an approximate calculation of the expected data rates in the different sections of the data path (quantities in paragraphs preceded by a § are assumed values, the others are computed). Buffers are assumed unlimited and no electronic limitation is taken into account, no safety margin is included.

Here we go:

§ the maximum CMS Level 1 trigger rate will be 100 KHz, with a usual Poisson distribution; events closer than 3 clock cycles are not permitted.

§ PACE output : each event has 3 samples per channel (maybe programmable ??) which are emitted by the PACE at the rate of 20 MHz

§ the A/D converts to 12 bits at a rate of 20 MHz

- the input rate to a K-chip from one PACE is: 1.5 [bytes] * 32 [channels] * 3 [samples/event] + 1 [address byte] + 2 [TimeTag bytes] + 1 [flag byte] = 148 [bytes/event]

- with @100 KHz trigger rate this results in 14.8 [MB/sec] from the A/D converter into each K-chip

- combining 4 PACE chips into one K-chip one has ~ 60 [MB/sec] into one readout link

- combining 16 readout links onto one FED one has ~ 960 [MB/sec] input rate

§ assuming a 4% occupancy and that zero suppression is done at the level of the FED, the FED output rate will be ~38.4 [MB/s]

- with 16 input links/FED this requires ~ 88 FED modules into ~ 4-6 crates

- The total data rate for the Preshower from the FEDs into the Event Builder will then be ~ 3.4 [GB/s]

3 The Readout System

3.1 Overview of the Preshower Readout System

The read-out electronics of the Preshower detector is based on a hybrid architecture consisting of a first analog pipeline stage where data are stored in analog form on tiny on-chip capacitors followed by an on-detector analog-to-digital conversion and a non-zero suppressed transmission of data to the Front-End-Driver cards. In the general CMS architecture the FEDs are in turn sending their data to the event builder.

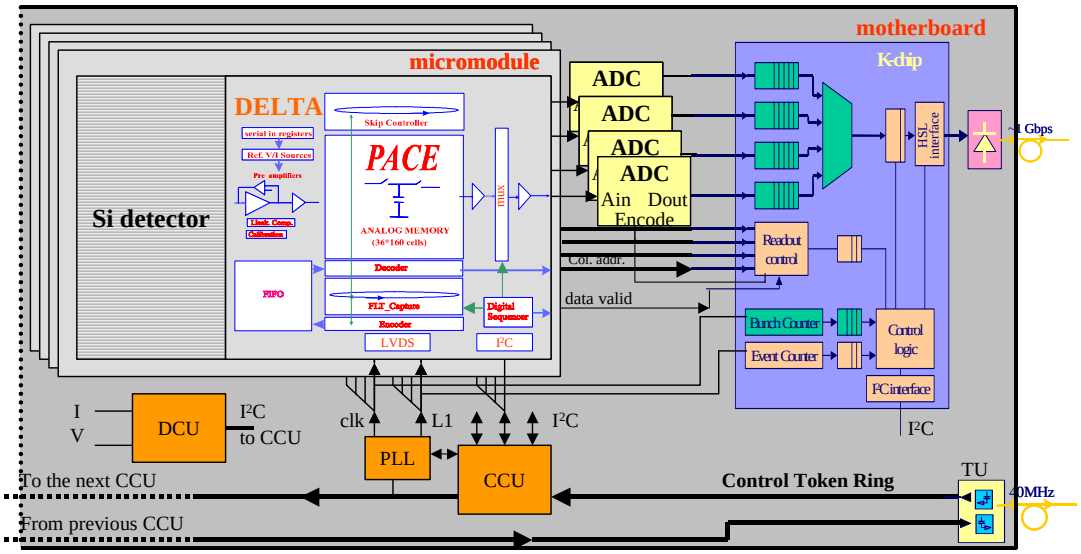


Figure 3.1 Block diagram of the Front End readout system.

3.2 The PACE chipset

The PACE chipset is the heart of the front-end system. It can read-out 32 silicon strips in parallel. The chipset is composed by two discrete ASIC components: a) the Delta chip and b) the PACE AM chip. Both chips will be implemented in the DMILL process.

3.2.1 The Delta chip

The chip consists of the following blocks:

- 32 low noise preamplifiers optimized used for the read-out of the silicon strip detector
- 32 signal shapers
- a number of programmable DACs used to set the bias conditions of the preamplifiers and shapers
- a calibration pulse control circuit

- a serial interface port used to give access to the programmable DACs and the calibration pulse control circuit

3.2.2 The PACE AM (*Analog memory*) chip

The chip consists of the following blocks:

- a 160 locations deep analog memory used to store the signal samples while waiting for the L1 trigger to arrive
- an output multiplexer used to scan all 32 analog memory locations once a read-out operation is started on a given column
- the control logic necessary to keep track of the locations where data have to be written and read to and from the memory, this logic also outputs the address of the column from where an event was stored once a read-out operation of the analog data is performed
- a number of DACs used to set the bias conditions of the analog circuitry
- an I^2C slow control interface used to program internal registers with configuration parameters and read status information
- an LVDS clock and trigger interface used to buffer these signals internally.

The ASIC chipset is currently being designed with a dynamic range of 12 bits (0.1 to 400 MIPS) and a linearity of XX %.

A simplified block diagram of the PACE ASIC chipset is shown in the Figure 3.2 below.

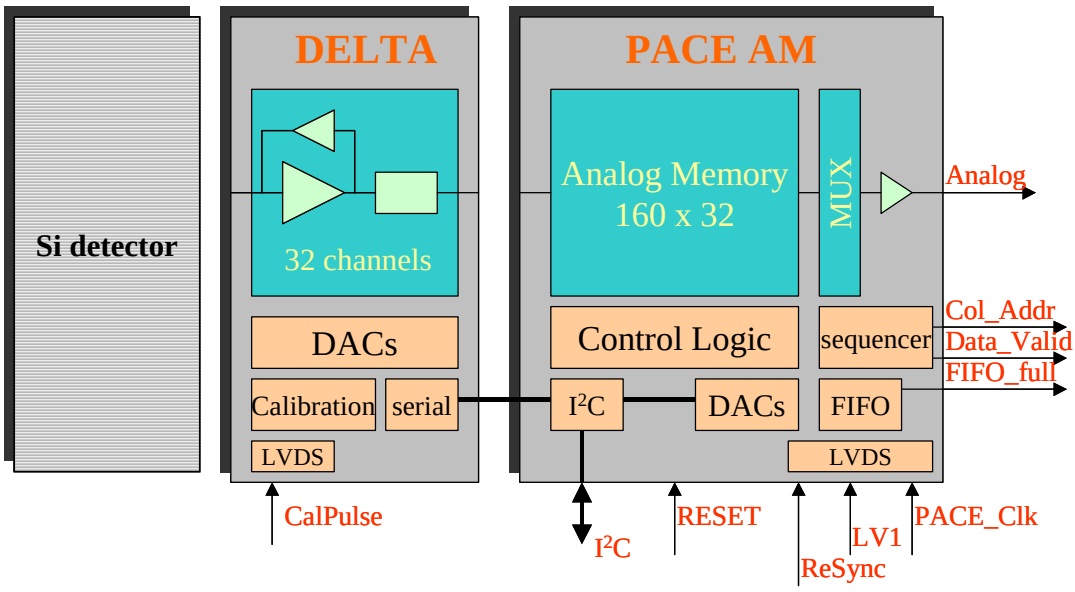


Figure 3.2 Simplified Diagram of the PACE chipset.

This diagram shows only the signals that participate in the interfacing with the Front-End Readout System. Table 3.1 below gives a brief description of these signals.

Table 3.1 Interface Signals of the PACE chipset.

Name	Type	Level	Description
Cal_Pulse	Input	LVDS	Calibration Pulse
PACE_Clk	Input	LVDS	Sampling Clock, 40MHz
ReSync	Input	LVDS	Pipeline & Sequencer Reset
LV1	Input	LVDS	Level 1 Trigger
Reset	Input	CMOS 5V	Resets all state machines
Col_Addr	Output	CMOS 5V	Serial Column Address output
Data_Valid	Output	CMOS 5V	Data Qualifier signal
FIFO_full	Output	CMOS 5V	Pipeline Overrun Flag
I^2C	Bi-Dir.	Open col. 2.5V	Slow Control port
Analog	Output	analog	DC coupling with the ADC

The PACE chipset has three distinct modes of operation as listed in

Table 3.2. the user changes the mode of operation using the control register in the PACE_AM chip (see Table 3.3). After power up the PACE enters immediately the SLEEP mode of operation. The PACE should then be operated according to the following flowchart:

POWER up -> SLEEP mode -> load configuration registers and verify -> bring PACE to the RESET mode -> enter RUN mode -> enter RESET mode -> enter SLEEP mode -> change values in the configuration registers -> enter RESET mode -> enter RUN mode …..

Table 3.2 PACE chipset Modes of Operation.

Mode	Description
RESET	Pipeline pointers are reset and the sequencer control signals are in a predefined state. This condition lasts as long as the ReSync signal is kept active. Any data stored in the pipeline are lost after entering this mode.
SLEEP	A minimum current biasing is applied on the preamplifiers for safety reason and to minimize power consumption on standby periods. The control logic is kept in a reset state.
RUN	Normal data taking mode. The pipeline pointers are running at the sampling frequency while the readout sequencer is enabled to readout stored events.

The following figures (Figure 3.3, Figure 3.4 and Figure 3.5) shows the timing diagrams of the fast timing signals driving the PACE chipset. The **ReSync** and **LV1** pulses have a duration of 25nsec while the **Cal_Pulse** (calibration pulse) should be at least 200nsec long.

For channel calibration purposes the Delta chip is equipped with a calibration circuit that can generate and inject current pulses of programmable total charge into selected channels. The channel selection is done by programming a mask register through the I^2C interface. The amount of the injected charge is analogues to the charging voltage of the calibration capacitors. This voltage is set by an on chip programmable DAC. The **Cal_Pulse** signal controls the switch that connects and disconnects the calibration capacitors on the channel input. The phase delay of this signal in respect to the sampling clock is crucial since it controls the distribution of the injected charge between subsequent samples. **The problem of the control of the calibration pulse phase delay is not addressed yet in our system.**

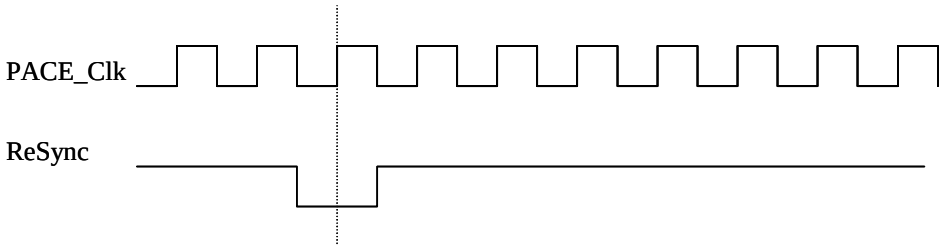


Figure 3.3 Timing Diagram of the ReSync pulse.

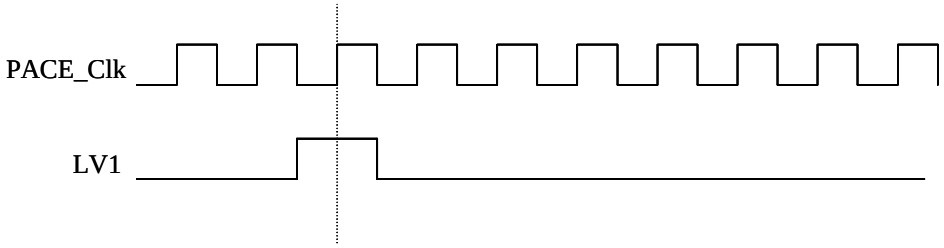


Figure 3.4 Timing Diagram of the Level 1 Trigger pulse.

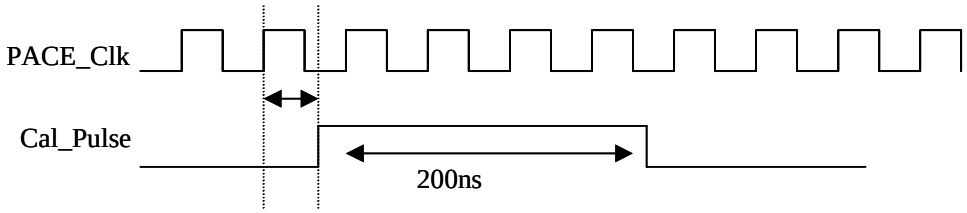


Figure 3.5 Timing Diagram of the Calibration pulse.

3.2.2.1 Readout Sequence

The following figures present three different phases of the readout cycle of an event from the PACE_AM chip.

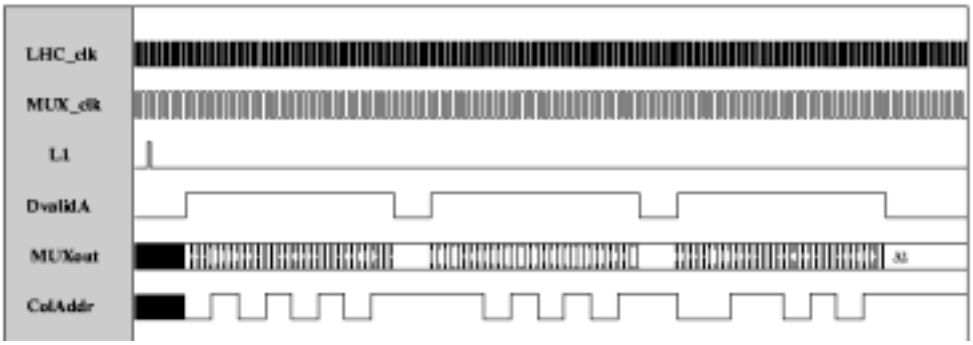


Figure 3.6 Complete Readout Cycle of One Event. (LHC_clk corresponds to the PACE 40MHz clock signal, the MUX_clk is a PACE internal signal.)

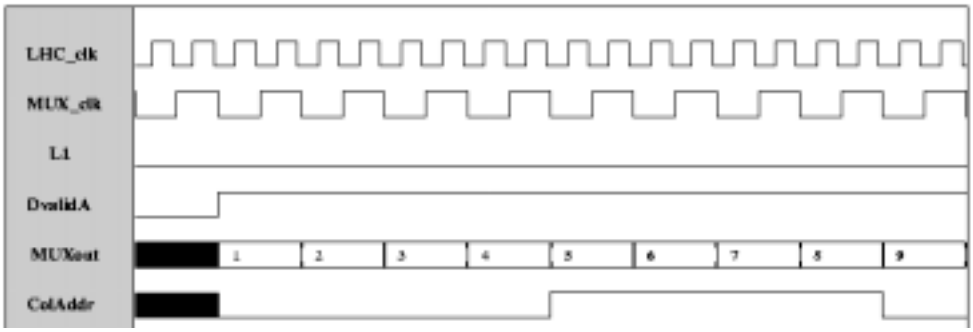


Figure 3.7 Header part of a Readout Cycle of One Event. (LHC_clk corresponds to the PACE 40MHz clock signal, the MUX_clk is a PACE internal signal.)

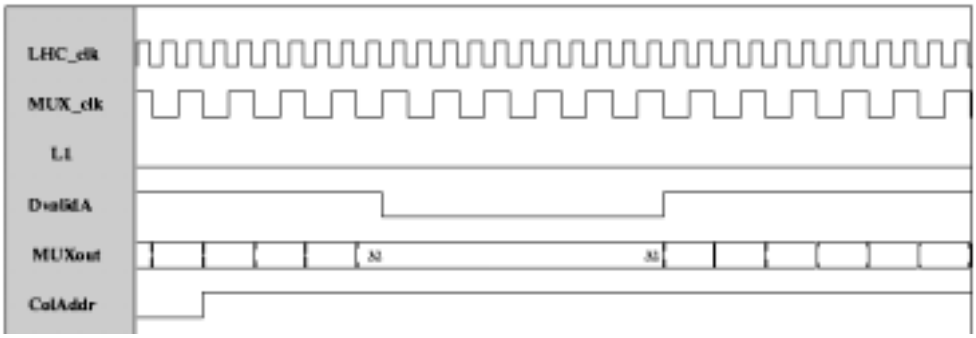


Figure 3.8 Intermediate part of a Readout Cycle of One Event, in between two consecutive columns. (LHC_clk corresponds to the PACE 40MHz clock signal, the MUX_clk is a PACE internal signal.)

3.2.2.2 I^2C Interface & Internal Registers

There is a set of configuration registers on both the Delta chip and the PACE_AM chip that can be accessed through a single I^2C line originating from the PACE_AM. The PACE_AM interface is a slave I^2C interface and complies to the PHILIPS I^2C standard V2.0. It accepts both 7-bit addressing and 10-bit addressing transactions on standard or combined format. It can also perform multiple byte transactions. **Most probably the 7-bit addressing is adequate for addressing the PACE chipsets installed on a motherboard. Multiple byte transactions will not be in use because this feature is not supported by the CCU (Communication Control Unit) master I^2C device.** For more Information the reader is referred to the "I2C-PACE" Internal note from AURELIA.

The name the location the address and the functionality of the PACE chipset internal registers is shown in Table 2.1 below.

Table 3.3 Internal Register Map for the PACE chipset.

I^2C Address	Chip	Name	Description
0	PACE_AM	**Control Reg**	Sets the modes of operation.
1	PACE_AM	**Latency**	Sets the trigger latency.
2	PACE_AM	**IreadAmp**	Sets a bias condition.
3	PACE_AM	**ISF**	Sets a bias condition.
4	PACE_AM	**Vadj**	Sets a bias condition.
5	PACE_AM	**IoutBuf**	Sets a bias condition.
20	Delta	**Control Reg**	Sets the Gain, Calibration mode and calibration precision.
21	Delta	**CalChanReg1**	Sets calibration mask for channels 1~8.
22	Delta	**CalChanReg2**	Sets calibration mask for channels 9~16.
23	Delta	**CalChanReg3**	Sets calibration mask for channels 17~24.
24	Delta	**CalChanReg4**	Sets calibration mask for channels 25~32.
25	Delta	**CalV**	Programs the calibration charge.
26	Delta	**Iin**	Sets a bias condition.
27	Delta	**DelatPC**	Sets a bias condition.
28	Delta	**LccRef**	Sets a bias condition.
29	Delta	**Ishaper**	Sets a bias condition.
30	Delta	**ShaperRef**	Sets a bias condition.

For more information about the PACE chipset and its operation the reader is referred to the forthcoming "PACE users manual".

3.3 The Analog to Digital Converter

A commercial Rad-Hard analog to digital converter will be used for the conversion of the PACE analog signal output. This converter is the Analog Devices AD9042, which is used in large quantity in the ECAL electronics.

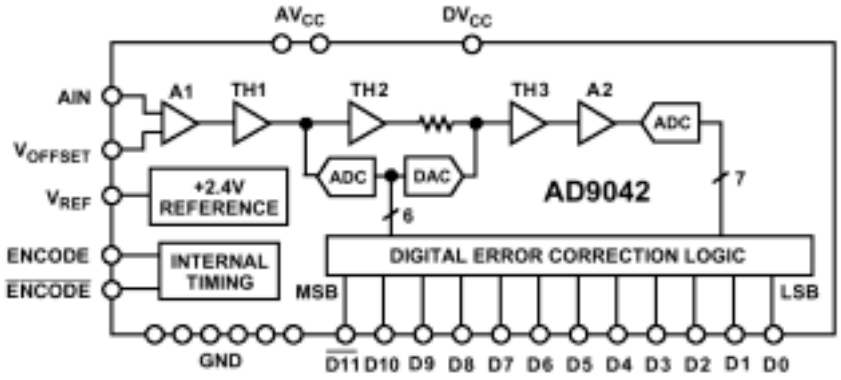


Figure 3.9 Functional Block Diagram of the ADC.

The AD9042 is a high speed (**41MSPS**), low power (**600mW**), **12-bit** analog-to digital converter. It runs off of a single +5V supply and provides CMOS compatible digital outputs. The AD9042 is built on Analog Devices high speed **bipolar process** (XFCB).

The analog input range is $1V_{p-p}$ centered at 2.4 Volts in reference to the ground potential. The input resistance is 250ohms and the capacitance is 5.5pf.

The conversion clock signal of the AD9042 is applied on the ENCODE terminals and can be driven from either single ended or differential sources. A differential signal source should have minimum nominal amplitude of 1.2V centered at 1.6V from ground. Clearly this input is not LVDS compatible and a **special output pad for the K-chip** has to be designed in order to drive properly this signal. The signal that drives the ENCODE terminals should be clean and free from jitter as excessive jitter limits the signal to noise ratio.

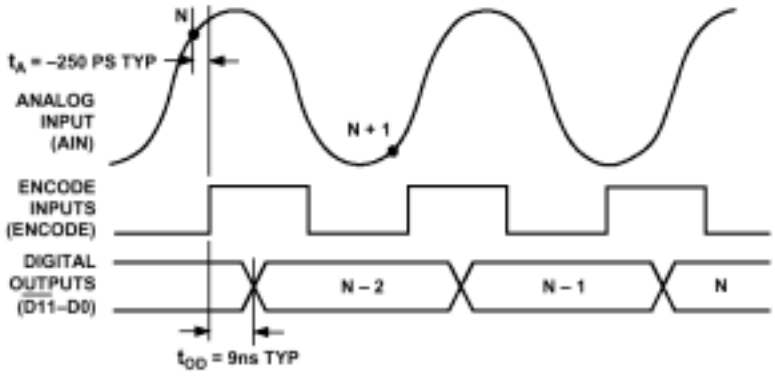


Figure 3.10 AD9042 timing diagram.

The AD9042 employs a two stage sub-range architecture giving rise to **two stage pipeline operation**. The timing diagram if the conversion operation of the ADC is shown in Figure 3.10. The digital output is **two's complement** coded.

For more details on the AD9042 specifications, theory of operation and application the reader is referred to the AD9042 data sheet from Analog Devices.

3.4 The K-chip

3.4.1 Functional Description

The K-chip function is to gather data from four PACE chips and format it in a way suitable to be sent over the high-speed digital link. As no data reduction occurs in the front-end system, the K-chip has to cope with the data rates produced by the PACE front-ends; this is detailed in the following sections.

The K-chip receives data in parallel from the PACE chips, builds a packet in a format suitable for the high-speed serial link and sends this to the remote FED cards.

While preparing this data block the K-chip adds some more information to it such as:

- the event number tag
- the bunch counter tag
- CRC information
- error information, if necessary

As the input data comes in 12 bit format, the K-chip aligns the data in contiguous blocks of 16 bits as to maximally utilize the link bandwidth. The data analysis engine in the FED cards will have to unpack the data into 12 bit wide words.

The dataflow used is a simple push type architecture. All K-chips in the system are synchronous and transmit data along their link at the same time, as no data reduction is performed until the FEDs level. Event data prepared in the output buffer of the K-chip are sent to the serial link transmitter. To simplify the system and reduce its cost this link is unidirectional and without flow-control. This means that whenever an error occurs in the transmission medium (either the serializer, the link itself or the receiver) a block of data belonging to one (or potentially even more) event(s) is irremediably lost. As another consequence, the FED has to be able to regain synchronization when one of the K-chips or links is sending data under some error condition.

3.4.2 Block Diagram

A simplified block diagram of the K-chip in the read-out system is shown in Figure 3.11.

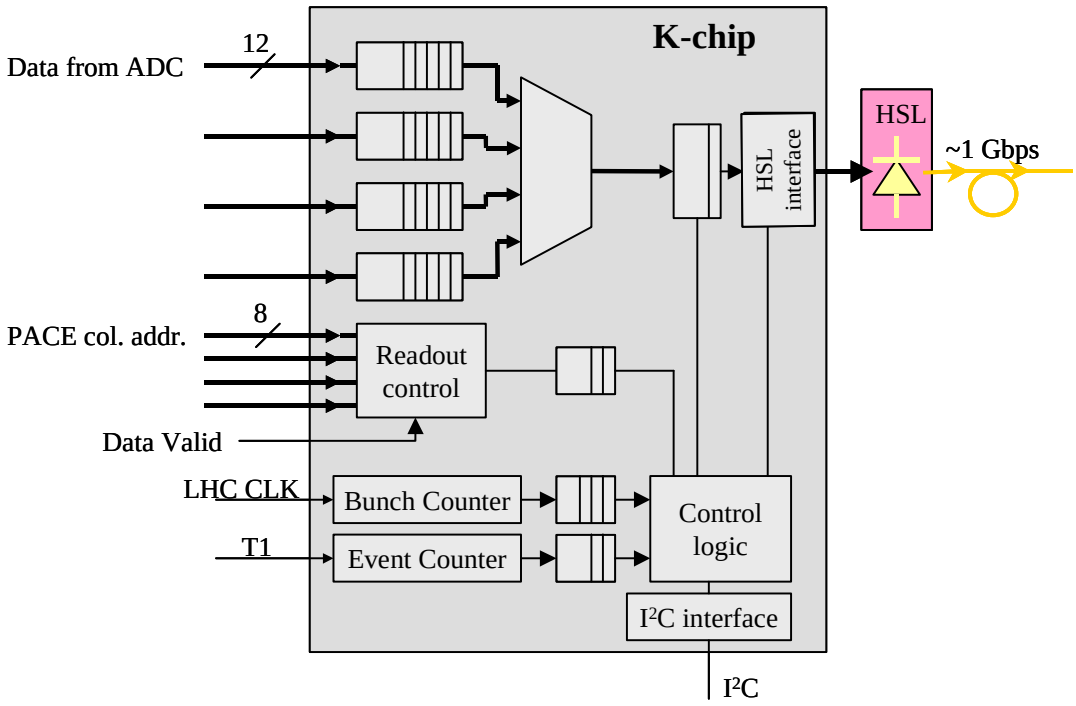


Figure 3.11 K-chip block diagram.

The K-chip consists of the following elements:

- four FIFO buffers, one per input channel. These are 12-bit wide FIFOs and several event deep, see below.
- A multiplexer used to scanm the four input FIFOs when a complete event has to be assembled in the output FIFO. This multiplexer also aligns the 12-bit wide data to 16-bit wide format.
- an output buffer, 16-bit wide, where the packet of data corresponding to an event is built before emission to the optical link
- a bunch counter used to count continuously the incoming 40MHz clock.
- an event counter used to count the number of incoming LV1 triggers.
- a trigger FIFO used to store incoming triggers while the readout of a previous event is in progress
- a control logic to provide the synchronization of the entire ASIC and the supervision of the sequence of operations necessary to build an event in the output buffer.
- a set of user register, accessible through the chip's slow control port (I^2C). The use of these registers are to control and read back status information from the K-chip. They provide also the possibility to the user to write some pseudo-event data into the data FIFOs to test the functionality of the readout chain.

- an I^2C based slow control interface used to access the K-chip internal registers and data FIFOs.

The simplified protocol followed by the K-chip to assemble one event into its output buffer is the following:

- the K-chip monitors continuously the state of its trigger FIFO
- when a trigger is pending in the trigger FIFO, it extracts it together with the bunch counter tag which was stored in it at the moment of the arrival of the trigger signal and stores this in the header of the outgoing data packet in the output FIFO with the K-chip ID number
- the data blocks at the head of the four input FIFOs are read and moved into the output FIFO
- a CRC is computed and appended to the event data packet
- the output is enabled and the packet is streamed out to the serial link.

3.4.3 Operation Modes

The K-chip can be initialized in two modes:

- normal read-out mode
- link test mode

In the first mode, the K-chip assembles event blocks as described above and it used in the normal data acquisition chain. In the link test mode, the K-chip can send out data which can be written into its input FIFOs via the slow control interface. This mode is used essentially as an aid to debug a malfunctioning link outside of the normal data acquisition mode.

3.4.4 Buffer Sizes

The size of the input buffer in the K-chip determines the probability of losing an event (inhibited by the trigger supervisor) because of a momentary congestion of triggers. Using an analytic model of the system we have determined that a buffer of 1.6 Kwords (corresponding to about 13 events) gives an event loss probability of less than 10^{-8}.

The output FIFO only needs to contain one event (~4*148 + overhead = 600 bytes) as no multi-event output buffering is provided.

3.4.5 Error Conditions / Error handling

3.4.6 Link Data Packet Format

The format to be used to send data through the High Speed Link is shown in Figure 3.13. Data words are 16-bit wide.

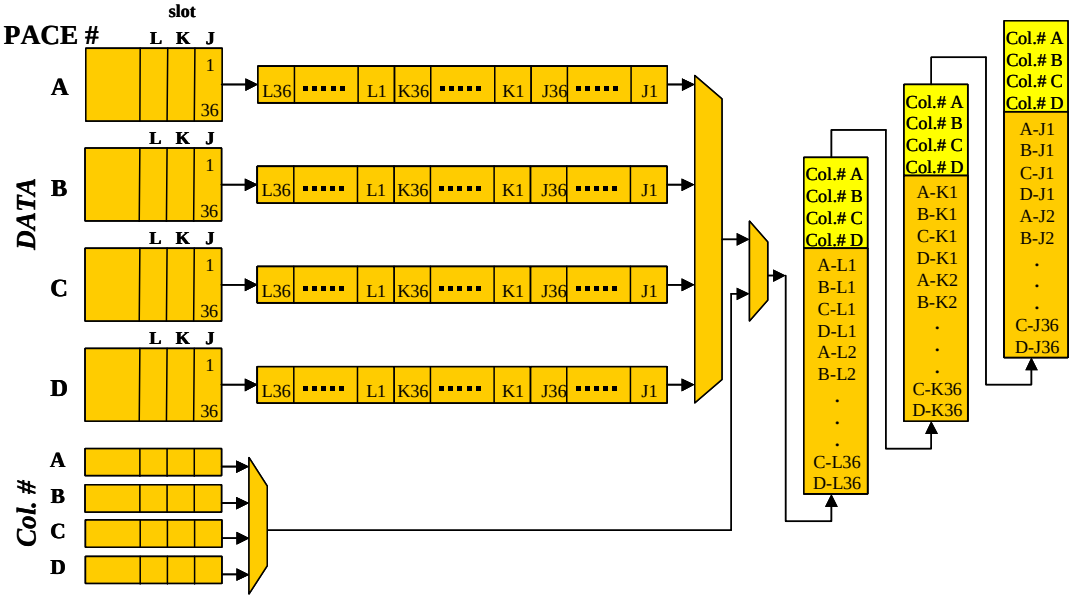


Figure 3.12 Mechanism for the Event Data Formatting.

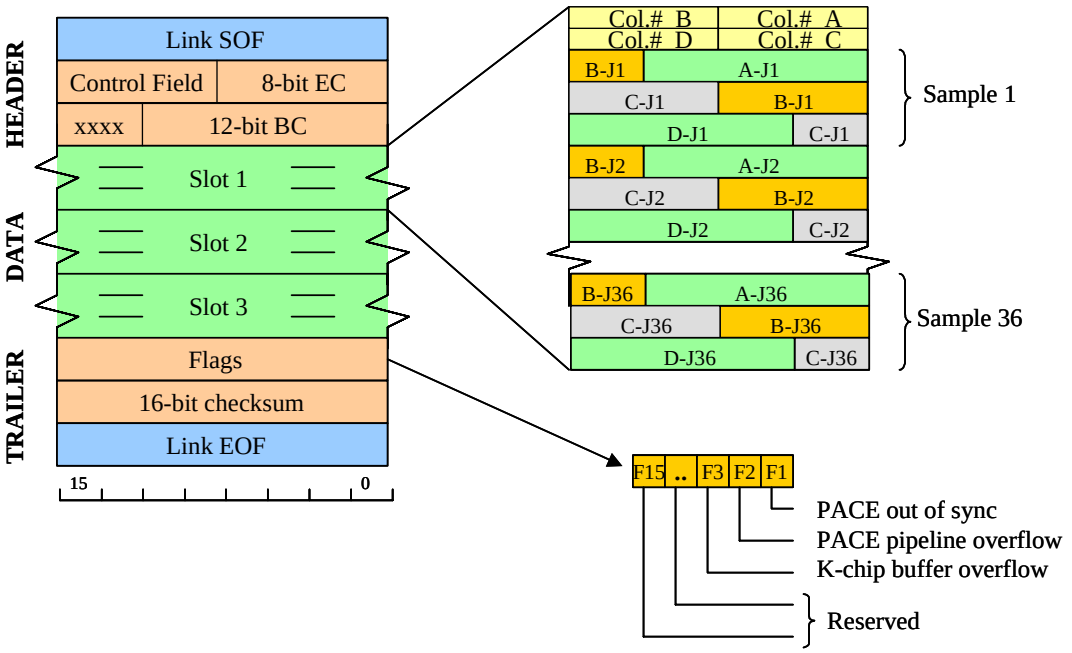


Figure 3.13 Link Data Packet Format.

The Link Data Packet starts with a Header Field followed by the Data Payload and ends with a Trailer Field.

The Header Field consists of:

- a Start Of Frame (SOF) word which is used to synchronize the readout operation

- a Control Field of 8-bits for signaling the type of Data Packet
- an 8-bit Event Counter (EC)
- a 12-bit Bunch Counter (BC)

The Data Payload Field consists of 3 identical data packets each containing information coming from a time slot. Each time slot data packet contains:

- the column addresses of the 4 PACE chips
- the 12-bit digitized values of the 36 data samples contained in one PACE column.

The Trailer Field consists of:

- A 16-bit word containing status flags
- A 16-bit Cyclic Redundancy Checksum word as calculated over the whole information in the data packet except the SOF and EOF words. The CRC field is calculated following the CRC-16 algorithm.
- An End Of Frame (EOF) word, which is used to signal the end of the data packet.

The size of one slot in the Data Packet can be calculated as follows:

(4 PACEs x 36 samples x 12-bit) + 2 words (*column address*) = 1,728 bits or 108 words of 16-bit.

The size of the Data Packet is then calculated as:

3 words (*Header*) + (3 slots x 110 words) + 3 words (*Trailer*) = 337 words.

3.4.7 I^2C Interface

3.4.8 Internal Registers

The Table 3.4 specifies the registers (all 8-bit wide) accessible via the I2C interface in the K-chip (double registers are tagged with a _H-L name).

Table 3.4 K-chip Internal Registers

Name	I^2C Address	Function	Type
CONFIG	0	This register contains various configuration and mode fields as specified below	R/W
ECONFIG	1	This extra-configuration register contains various configuration and mode fields as specified below	R/W
KID	2	K-chip ID register	R/W
Reserved	3		
STATUS	4	This register contains a number of status bits as specified below	RO
FIFOMAP	5	This register contains a pointer to one of the FIFOs in the chip, it is used to direct read/write operations to the corresponding FIFO	R/W
FIFODATA_H-L	6-7	When in Link Test mode, writing to this register causes data to be written into the FIFO pointed to by the FIFOMAP register; a read operation instead reads data from the corresponding FIFO. When in normal mode, read/write operations to this register are ignored	R/W
EVCNT_H-L	8-9	A read operation from this register gives the 16 bit current content of the Event Counter in the K-chip	RO
BNCHCNT_H-L	10-11	A read operation from this register returns the 16 bit bunch counter value used to tag the last event.	RO

3.4.8.1 The *CONFIG* Register

Table 3.5 *Config* register bit assignment.

Name	Position	Function
Mode	7	Determines if the K-chip is in normal or test mode. A 0 in this bit corresponds to normal mode A 1 in this bit corresponds to test mode. The bit is reset to 0 after an external reset to the K-chip.
	6	
	5	
	4	
	3	
	2	
	1	
	0	

3.4.8.2 The ECONFIG Register

Table 3.6 *ECONFIG* register bit assignment,

Name	Position	Function
CLPOS	7	Clear PACE-Out-of-Sequence: when writing a one to this bit, the K-chip clears all the POS bits in the STATUS register. This bit is read always as a 0.
	6	
	5	
	4	
	3	
	2	
	1	
STRSRT	0	Stream read-Out Start. When in Link-Test mode writing a '1' to this bit causes the K-chip to beahve as after having received a T1 signal in input, namely the input FIFOs are transferred to the output FIFO a data are emitted to the link. When in Normal Mode, writing to this bit has no effect.

3.4.8.3 The *STATUS* Register

Table 3.7 *STATUS* register pin assignment.

Name	Position	Function
GERR	7	General error. This is an OR of all error conditions in the K-chip
POS3	6	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 3 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS2	5	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 2 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS1	4	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 1 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS0	3	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 0 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
	2	
	1	
	0	

3.4.8.4 The *FIFOMAP* Register

Table 3.8 *FIFOMAP* bit assignment.

Bits <2:0>	Map
0 0 0	R/W operations to input FIFO channel 0
0 0 1	R/W operations to input FIFO channel 1
0 1 0	R/W operations to input FIFO channel 2
0 1 1	R/W operations to input FIFO channel 3
1 0 0	R/W operations to output FIFO.

3.4.8.5 FIFODATA Register

This 16 bit register is used to write 12 bits of data into the FIFO pointer to by the FIFOMAP register. The write operation actually occurs when the FIFODATA_L register is written. A read operation reads the last in the FIFO and decrements by one the number of words in it.

3.4.8.6 EVNCNT Register

This read-only registers return the value of the Event Counter associated with the last occurrence of a Level 1 trigger

3.4.8.7 BNCHCNT Register

This read-only register returns the value of the Bunch Counter associated with the last occurrence of a Level 1 trigger.

3.4.9 Packaging

3.5 The High Speed Link

3.5.1 Link Requirements

The realization of the Preshower Readout System requires the availability of a high-speed digital optical link between the detector front-end electronics and the FED VME modules. In general, this link should be unidirectional having a sustained data transfer rate in the range of 1 Gbps. The transmitting side of the link (electronics and optoelectronic components), located on the detector, has to be radiation resistant up to the total dose radiation levels required for the Preshower electronics. The cooling of the detector imposes also some constrains in the electrical power dissipation of the transmitting side. The power dissipation has to be kept around 0.3-0.5W/link.

In the Preshower Readout System we can use a link that operates either synchronously or asynchronously to the LHC clock. Synchronous links are capable of transmitting one word of data at each LHC bunch crossing and are usually needed for sending information to the trigger system. Asynchronous links work in a block transfer mode, where a certain amount of data is buffered in the transmitting end, gets properly formatted and then shipped to the destination in a block form. Since in the Preshower Readout architecture the derandomizing

buffers are located on the detector before the K-chip there is no constrain to use a synchronous link. Both types are equally acceptable.

3.5.2 Transmitter Interface

The output of the K-chip will be directly connected to the High Speed link. It is not foreseen to have any "glue" electronics in between. It is of particular importance to pay attention not only on the functional aspects of the link but also to the electrical level compatibility of the K-chip and the link interface.

The link operation should be completely transparent to the K-chip. This means that it should be capable to maintain bit synchronization and word synchronization without any external intervention.

3.5.3 Receiver Side of the Link

There are no demands of radiation hardness in the receiving side of the link hence there is no reason to use custom made electronics. The receiving side of the link should use commercially available components to keep the cost of the links low. A possibility would be to have a combination of commercially available deserializers with some amount of logic implementing the protocol functionality embedded in an FPGA. Board space on the PCB and power dissipation should be taken into consideration when designing the FED module and choosing the multiplicity of optical links serviced by a FED module.

Table 3.9 High Speed Link Transmitter general requirements.

Item	Specs
Transfer Rate	~1 Gbps
Fiber Type	
Laser Wavelength	
Fiber Length	~120 meters
Interface Clock Frequency	40.08 MHz (LHC clock)
Temperature Range	-15 °C to 50 °C
Power Supply	
Max Power Dissipation	
Interface Electrical Levels	CMOS compatible
Radiation hardness	> 10 MRad, 2×10^{14} n/cm ^{2} in 10 years of operation

3.6 Synchronization with CMS DAQ and Trigger system

This section describes the general trigger synchronization philosophy used for the Preshower read-out. Only the normal 'physics' triggers are described:

- Triggers are received from the general CMS trigger system by the trigger supervisor; if there is no current congestion in the front-end buffers the trigger supervisor forwards the trigger to the Preshower FECs which transmit it to the front end chips using an optical 40 MHz link.

- As no data reduction occurs in the front end, the data acquisition system runs synchronously in the PACE and K-chips. After the system has been synchronously initialized to a know state, all PACE and K-chips should always be in the same state (i.e. identical buffer positions and pointers at a given clock cycle) during a run. This makes relatively easy to build a PACE and a K-chip emulator in the trigger supervisor. The data acquisition becomes asynchronous after the FED stage, as different FEDs will store different amount of data on an event-by-event basis.

- The K-chips keep monitoring the state of the PACE pointers by reading the pointer position on the ColAdd lines for each event and comparing these between the different PACE chips and with the internally kept trigger counter.

- The K-chip has an input buffer for incoming triggers; should a trigger be delivered during the read-out of a previous event, the K-chip stores it in a queue until the data can be read from the PACE chips. The PACE implements the same queue. Neither the PACE nor the K-chip need to make sure that the minimum delay of three clock cycles is provided by the trigger system. This is done by the trigger supervisor.

- The system runs smoothly until an error or a congestion occurs. A few possible error situations are described below, but this list is far from being exhaustive:

  - PACE chips get out of sync: this situation is recognized by a K-chip which notices that for a given event the data block from a PACE chip is coming with a different address tag (ColAdd). Here the K-chip builds a special error packet and transmits it to the FED. Once this packet has reached the Preshower event-builder, action must be taken to reset the chain concerned.

  - The trigger supervisor receives an L1 trigger when the emulator tells it that the PACE or the K-chip have reached the high watermark level. The trigger supervisor suppresses the trigger to the front end chips but still sends the information that an empty event has to be built by the FEDs.

  - A front end PACE receives a trigger when its buffers are already at the high watermark, i.e. the trigger supervisor for some reason has failed to inhibit this trigger or a spurious trigger signal was created by electronic noise or SEU in the ASICs. The PACE should signal an error condition to the K-chip in the output address lines ColAdd and ignore the trigger.

  - A K-chip receives a trigger when its buffers are already at the high watermark, i.e. the trigger supervisor for some reason has failed to inhibit this trigger or a spurious trigger signal was created by electronic noise or SEU in the ASICs. The K-chip should signal an error condition by sending an error data packet to the FED and ignore the trigger.

3.6.1 Synchronization signals

Basically two signals are necessary to keep the entire pre-shower system in sync. These are:

- the 40 MHz clock signal as recovered from the PLLs in the system from the merged CLK+T1 signal

- the encoded trigger signal, also recovered from the PLL.

The encoded trigger signal is qualified by the rising edge of the clock

The encoded trigger uses three consecutive bits in the T1 stream to specify different conditions according to the following table:

Pattern	Command
100	LV1A (Trigger Level 1 Accept)
110	Test Pulse (Calibration)
101	Reset (Reset FE Pipelines)
111	BC0 (Bunch Crossing Zero identifier)

Table 3.10 Trigger signal coding

The T1 is distributed using two coding systems; in the TTC system the channel A is used to encode it, in the FEC-CCU system it is mixed with the CLK.

The above coding allows for four type of signals to be transmitted (using a sequence of three bits). All front-end ASICs receiving the T1 signal have to wait three cycles before performing a complete decoding of the signal, thus extending the pipeline delay by three clock cycles. The timing for the distribution of these signals is determined by the chain of:

- the central CMS trigger system

- the first level distribution over the TTC network

- the preshower trigger supervisor

- the second level TTC system

- the FEC-CCU distribution network

- the PLLs on the front-end modules.

The signals are explained in the following paragraphs.

3.6.1.1 Normal Physics Trigger

The normal physics trigger is used in the PACE to tag the memory location corresponding to the arrival of the trigger (a programmable latency is configured in the PACE) and to initiate a read-out operation of these memory cells. The same signal is also used in the K-chip to alert that an event will be coming from the PACE.

3.6.1.2 Calibration Trigger

The calibration trigger sequence is used to flag special calibration events. The details of such events still has to be determined.

3.6.1.3 General Reset

This is a very important synchronization signal as it is used to bring the entire system in a known state. Upon arrival of the General Reset the following operations have to be performed:

- in the PACE
  - reset the read and write memory pointer to a known value
  - reset the pointer FIFO
  - etc.
- in the K-chip
  - reset the Event Counter
  - reset the Bunch Counter
  - clear all FIFOs and their pointers
  - reset all error conditions
  - etc.
- in the FED
  - clear all buffers
  - reset all counters to a know value
  - etc.

This signal is generated at the beginning of each run.

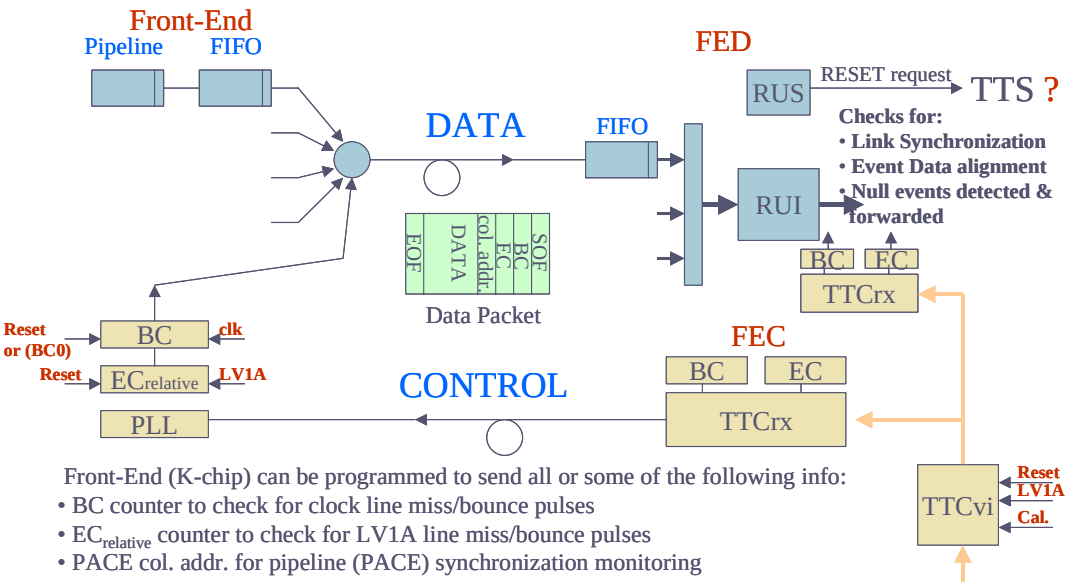
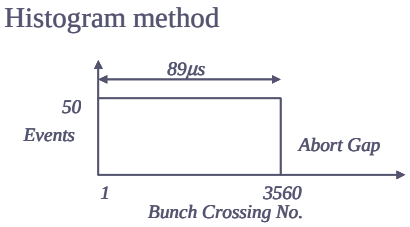


Figure 3.14

3.6.2 Bunch Crossing Identification



Probability of a non-zero event at low luminosity ……. $3*10^{-3}$
Say 50 entries per bunch crossing,
3560 bunch crossing per 89us
We therefore need $6*10^{7}$ events > 800 s (with 75kHz LV1A)

This assumes :
** Good S/N (High gain mode)*
** Histogram at the full rate (75kHz)*
either in the DAQ
or by a μp in the FED (we would need a bunch crossing no. for each trigger).

Figure 3.15 Histogram method for Bunch Crossing identification.

3.6.2.1 Requirements for clock jitter

The charge measurement accuracy of the Preshower is approx. 5%. Charge integration in 3 time slots insensitive to jitter at the ns level. Voltage sampling with 3 samples, 30ns peaking time -> simulations show a 1ns jitter from one sample to the next gives ~ 2% error. Hence a jitter < 1ns p.p. is tolerable.

3.6.2.2 Requirements for clock Phase adjustments

- Preliminary simulations show that voltage sampling using 3 samples and a ±2ns phase variations has almost no impact on the charge measurement.
- The step size of the PLL is 1ns. This is good enough for the Preshower.
- The phase will be scanned in 1ns steps to correctly position detector pulses.
- We do not expect to have to adjust the clock phase often.

3.6.3 Synchronization Procedure

Use the histogram method as mentioned above. Correlate a large energy deposition in the ECAL (a few GeV) with the Preshower to verify the synchronization of the system.

3.6.4 Loss of synchronization

3.6.4.1 Buffer Overflows

3.6.4.2 Spurious pulses on Fast Timing distribution system

3.6.5 Recovery from Synchronization Loss

The FED detects sync. loss by checking:

- the buffer full error flags of the event data packets and
- the time stamps on the event fragments (BC number, Event Number, PACE column addr.)

We would like to have the possibility of applying a Front-End electronics reset signal in 1/x abort gaps. The period of reset (x) would depend on the stability of the system.

4 The Control System

4.1 Overview of the Preshower Control System

The tasks of the Preshower Front-End Control System are to distribute to the detector embedded electronics:

- Fast Synchronizing signals and timing information (LHC clock, L1 trigger, Reset etc) and
- Slow control information for controlling the status of the detector, monitoring of environmental parameters, front-end electronics set-up and calibration and downloading of operating condition parameters.

The Preshower Front-End control system is a derivative of the CMS Tracker control system and re-uses the ASIC and optoelectronic components initially developed for the Tracker control system.

4.1.1 Control System Architecture

The FE control path is functionally separated from the Data Acquisition (FE readout) path, allowing the detector and the embedded electronics to be monitored and controlled also when the more complex DAQ system is unavailable.

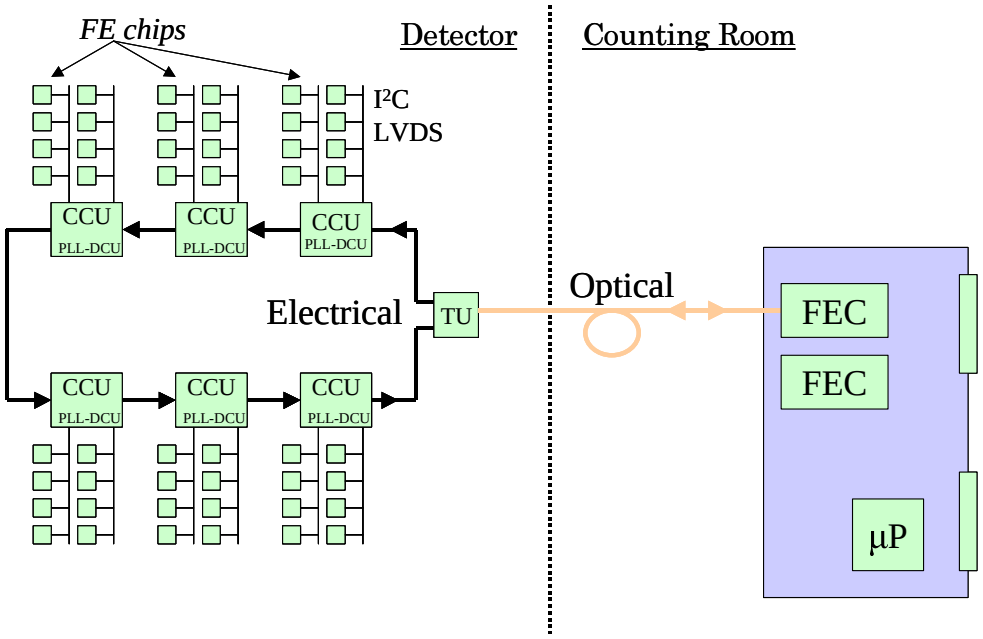


Figure 4.1 Overview of the FE Control System.
(CCU : Communication Control Unit,
DCU : Detector Control Unit, TU : optical Transceiver Unit).

The Preshower FE Control System architecture is shown in Figure 4.1. The system design is a careful balance between a long distance optical network and a local electrical. The long connection (>100m) between the control room and the first *patch-panel* mounted on the detector uses optical fibers. To minimize the cost and

to keep the power dissipation low the ring connection on the detector itself uses electrical signals with Low Voltage Differential Signaling (LVDS) levels.

The FE control system architecture is based on two layers:

- The first layer, called the **Ring Network**, connects the external Front End Controller (FEC) to a number of detector-embedded ASICS named Communication Control Units (CCU). There is one CCU chip on every detector electronics motherboard.

- The second layer, called **Channels**, connects the CCU chips to the Front End chips (PACE, K-chip) on the same motherboard.

In this architecture the control is done by sending data packets (called **messages**) to the respective channels, which interpret the messages as commands, execute some action onto the Front End chips (for example a read or a write operation) and return a status reply to the FEC via another message. The data transport protocol employed in the FEC – CCU system handles the remote devices that are controlled by the CCU as remote independent channels, each one with a particular set of control registers and/or allocated memory locations. The channels are completed separated from each other to allow concurrent operation on them. The remote channels can perform transfers to their end-devices in parallel. For more information on setting up and performing data transfers on the channels the reader is referred to the CCU documentation (see also the CCU section of this document).

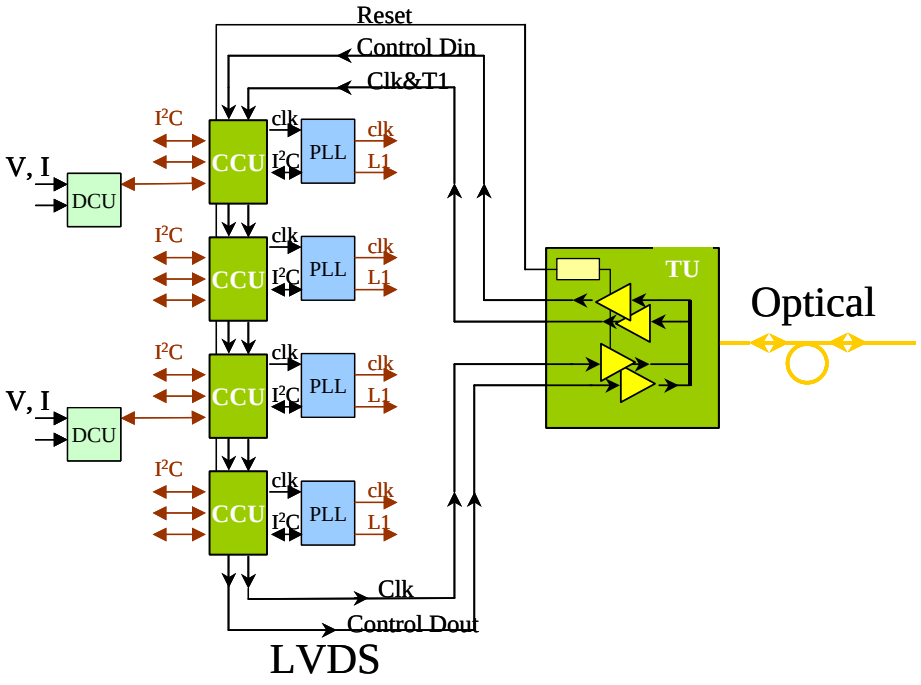


Figure 4.2 Overview of the FE electronics Control System

The physical implementation of the link uses two fibers for sending clock, trigger and data to the detector and two for the returning clock and data. Figure 4.2 shows the fiber arrangement of the FE control path. Separation of clock and data into two paths simplifies the amount of data and clock recovery electronics in the embedded environment. In this way the CCU ASIC can easily be integrated with a

fully digital component, without the need for clock regeneration PLL and data extraction and decoding circuit. Data synchronization is easily maintained because data are validated by the rising edge of the clock (see Figure 4.5).

On the other hand the CCU chip needs an external clock to run its state machines. This clock signal can be provided by the PLL chip used to regenerate the LCH clock and the L1 trigger as shown in Figure 4.2.

4.1.2 Redundancy in the Ring Network

To cover the most evident cases around the slow control, redundancy hardware has been added by doubling and intertwining all the connectivity between CCUs and doubling the optical links. Should a specific CCU fail, the architecture supports an alternate path going around the faulty node, which allows to keep the ring functioning. Such architecture is safe against all multiple failures, as long as there is no double failure in two adjacent CCUs. The scheme used in this approach is shown in the figure below. The ring monitoring and reconfiguration is handled completely by sending network management commands from the FEC.

Figure 4.3 shows the ring network redundancy schema in use. This schema requires that the CCU chips have two sets of input and output ports. The **primary port A** is the default port and is used in normal operation. The **secondary port B** is the auxiliary port and is used when there is a need to bypass a failing CCU chip on the ring.

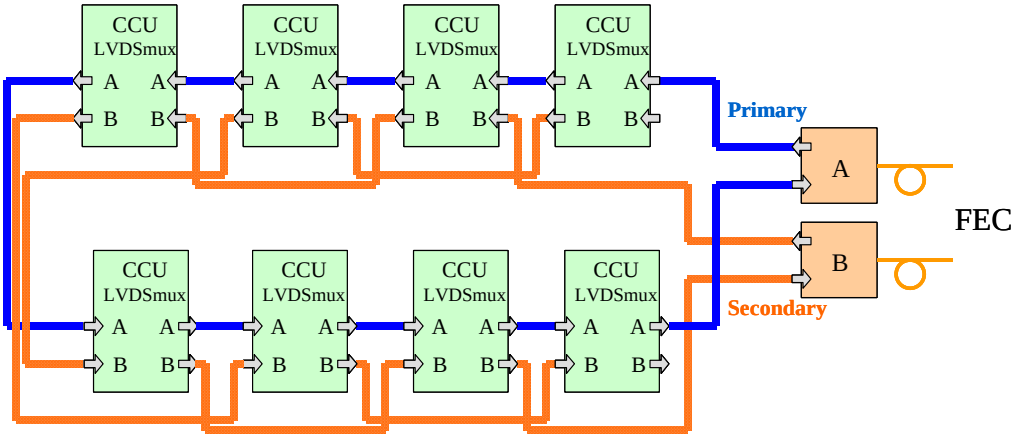


Figure 4.3 Ring Network Redundancy Schema.

Each port consists of two signals, one that carries the clock and LV1 trigger and another that carries the control data. Both signals have to be routed through the same path in the control ring. A small chip, called LVDSMUX, handles the routing of these two signals as shown in Figure 4.4. This chip is capable of rerouting two LVDS signals and is under the control of the CCU chip.

This redundancy schema uses two TUs (Transceiver Unit) to cover the case of a failure of one of these optoelectronic components and/or the failure of the first or the last CCU on the ring. As a consequence of this the number of optical fibres for the control links need to be doubled. Notice that the first and the last CCU in the ring have their B port unconnected.

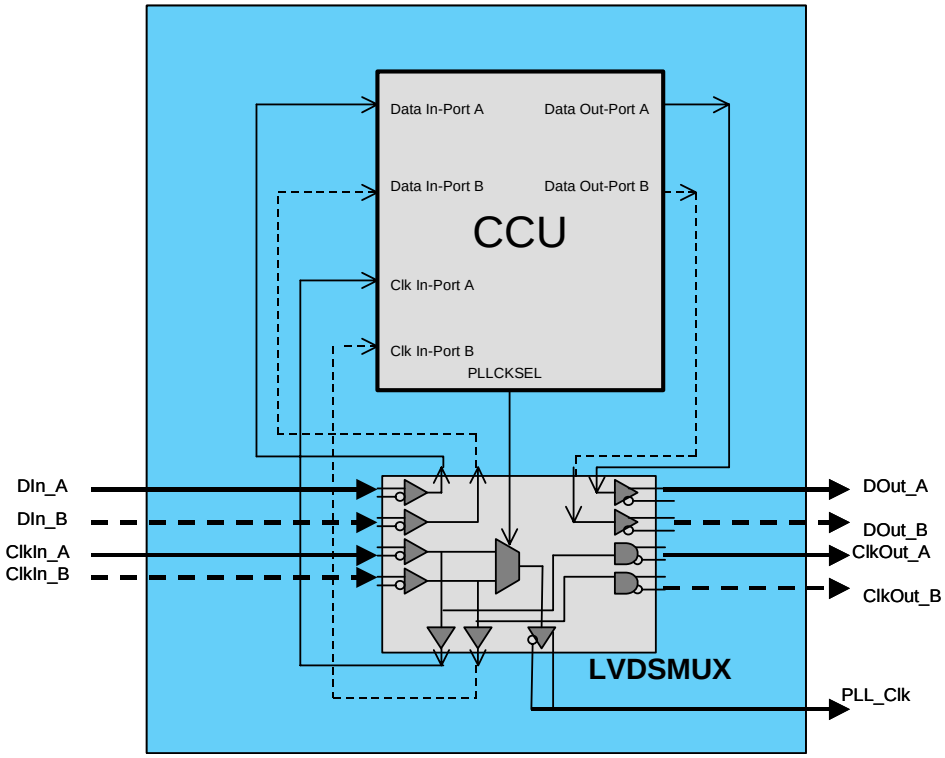


Figure 4.4 CCU-M cabling for redundancy.

The implementation of the control system with the presented redundancy schema is discussed in detail in section 5.3.2.

4.2 Fast Control Information

In this system, the LHC clock and the L1 trigger decisions are encoded and distributed as a single signal as shown in Figure 4.5. This signalling scheme minimizes the bandwidth and the power requirements if the transmission system.

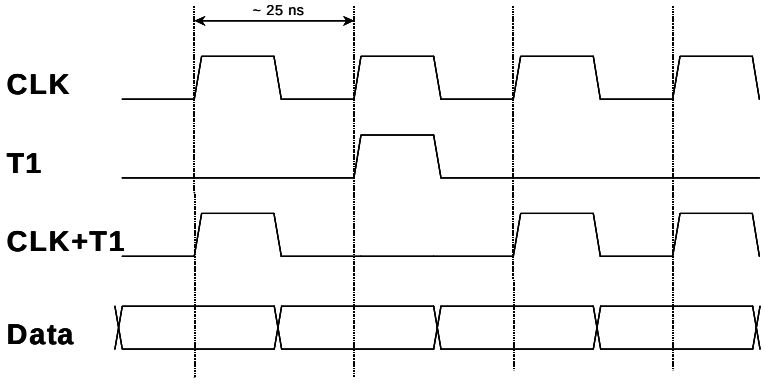


Figure 4.5 Clock and Trigger coding. Data timing.

Table 4.1 Trigger Commands

Pattern	Command
100	LV1A (Trigger Level 1 Accept)
110	Test Pulse (Calibration)
101	Reset (Reset FE Pipelines)
111	BC0 (Bunch Crossing Zero identifier)

4.3 Slow Control Information

4.3.1 I^2C Bus Distribution

The protocol is specified in detail in the Philips data books so there is no need to repeat here.

We are currently investigating two options for distributing I^2C channels on the motherboard level. These options are described below.

4.3.1.1 Option #1

This option uses only a few I^2C bus lines of the CCU chip. The remaining lines are left unconnected. A typical bus arrangement for a motherboard hosting 10 PACE chips is shown in Figure 4.1. Note, that the DCU chip shares the same I^2C line with the PACE chipset in the micromodule that is installed.

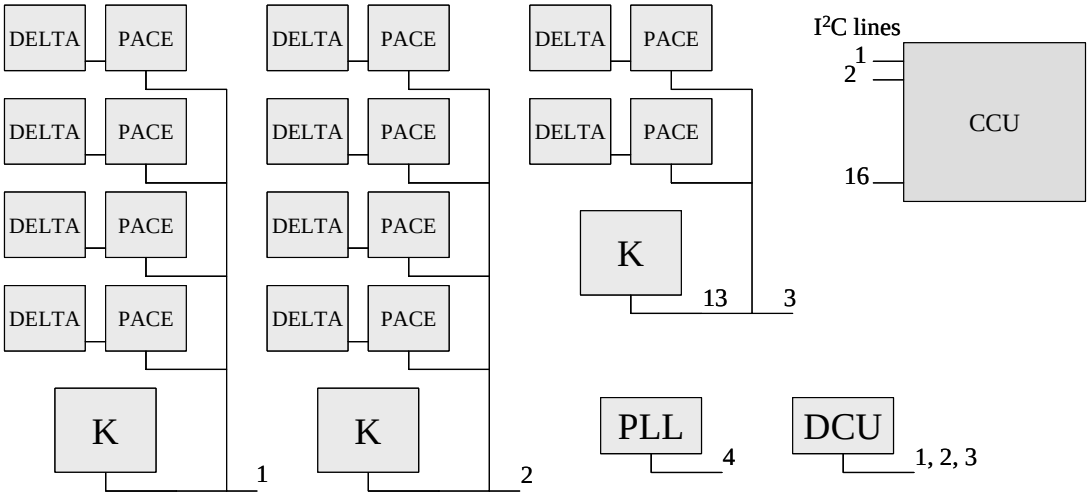


Figure 4.6 I2C bus distribution on the FE chips. Option #1.

4.3.1.2 Option #2

This option uses nearly all the I^2C bus lines of the CCU chip. The few remaining lines are left unconnected. A typical bus arrangement for a motherboard hosting 10 PACE chips is shown in Figure 4.2.

In this option we use one I^2C line per K-chip, one line per DELTA-PACE pair of chips, one line for the PLL chip. The DCU chip shares the same I^2C line with the PACE chipset in the micromodule that is installed.

This solution brings a level of redundancy in the I^2C bus distribution on the motherboard and its micromodules. If one bus line gets jammed by a failing chip the rest of the lines would remain operable.

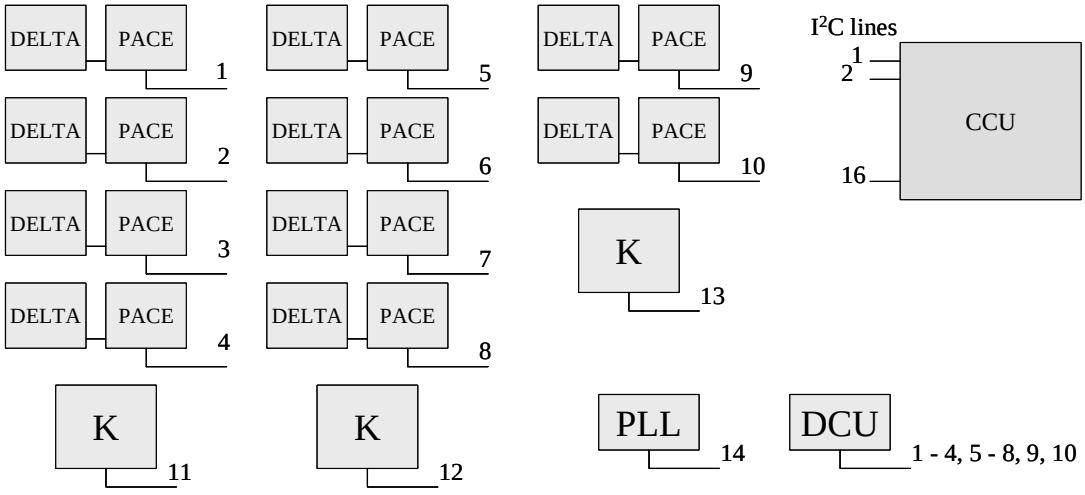


Figure 4.7 I2C bus distribution on the FE chips. Option #2.

Notice: One I^2C line should control devices connected on the same cluster. If the line fails then only this cluster gets affected and not others on the same motherboard.

4.3.2 I^2C Bus Transactions

4.3.2.1 Option #1

The data packet transaction format on the I^2C bus for option #1 is shown in Figure 4.3. Using a 7-bit addressing mode on the I^2C bus transaction makes the CCU capable to access up to 112 chips on every bus line and address 256 registers in each chip. This solution uses the combined I^2C bus transaction format.

Read Operation

S	Slave addr.	W	A	Register addr.	A	Sr	Slave addr.	R	A	Data	A*	P

Write Operation

S	Slave addr.	W	A	Register addr.	A	Sr	Data	A	P

Addressing mode: 7-bit
Slave addressing range: 112 chips
Register addressing space: 256 bytes
Transaction Format: combined
Transaction mode: single byte

Figure 4.8 Data packet format on the I2C bus for option #1.

4.3.2.2 Option #2

The data packet transaction format on the I^2C bus for option #2 is shown in Figure 4.4. Using a 7-bit addressing mode on the I^2C bus transaction makes the CCU capable to access one chip on the same bus line and address up to 112 registers in each chip. Two chips can share the same bus line if their register base address can be set appropriately so that there is not overlapping. This should be the case for the DELTA-PACE pair of chips. (I am assuming here that the DELTA chip has its own I^2C bus interface and is not controlled by an extension of the PACE I^2C interface. This solution uses the standard I^2C bus transaction format which is simpler to implement in the FE chips and makes transaction shorter and faster to complete.

Read Operation

S	Slave addr.	R	A	Data	A*	P

Write Operation

S	Slave addr.	W	A	Data	A	P

Addressing mode: 7-bit
Slave addressing range: 1(or 2) chip(s)
Register addressing space: 112 bytes
Transaction Format: standard
Transaction mode: single byte

Figure 4.9 Data packet format on the I2C bus for option #2.

Notice: This option cannot be used to control the PACE chipset (it does not accept this type of I^2C message format). This is only an option for the K-chip.

4.4 The CCU (Communication Control Unit)

4.4.1 Overview Description

This IC is the key component of the slow control system. On one side it interfaces to the Ring network performing the function of a node controller, running at 40Mbps, and on the other is a master for the local I^2C channels and memory busses used to access the intergraded circuits. A block diagram of the CCU is shown in Figure 4.10.

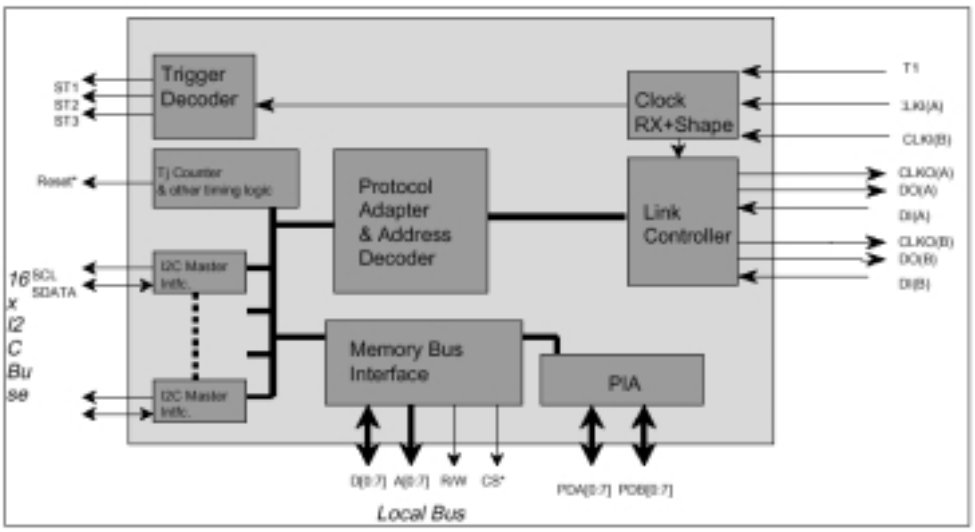


Figure 4.10 Block diagram of the Communication Control Unit (CCU).

The CCU interfaces to the network via two sets of network ports, each 4lines wide. Two sets are used for redundancy. Normally only one set is operating. The CCU can receive commands from both input ports, and switches to one or the other set upon reception of a command coming from the previous CCU in the ring or from the FEC, when a network supervisor realizes that a given network path is broken.

The CCU contains 16 master I^2C interfaces conforming to the standard and to the extended I^2C protocols. A generic synchronous memory bus master interface with 8-bit address lines and 8-bit data lines operating at a programmable speed is also present. In addition 16 I/O lines with programmable direction are provided through a parallel interface similar to the one used in popular micro-controllers. These lines can be used to control switches and monitor external digital lines.

Finally the CCU contains a simple programmable logic block to decode the Trigger Commands on the Ring Network "clk-T1" line. The CCU chip supports one, two, or three missing pulses in the clock signal stream. One missing pulse normally encodes to level 1 trigger command while the rest of the sequences can be user defined. In the Preshower control system the assignment of the valid Trigger Commands are shown on Table 4.1. These Commands are decoded on four individual output signals in the CCU chip.

More information concerning the functionality and operation of the CCU can be found in the "CCU, Communication and Control Unit ASIC for Embedded Slow Control", A. Marchioro, Draft document, 5/27/98.

4.4.2 ASIC Design Status (December 13, 2000)

A CCU module (called CCUM) that emulates the functionality of the CCU exists and is available to users. The module uses a non Rad-Hard prototype of the ASIC in a 5V technology. The module uses voltage level translators on the I/O pins of the ASIC in order to interface correctly with the 2.5V environment.

A radiation Tolerant version of the CCU ASIC is under development. The chip is scheduled to go for submission late February 2001.

4.5 The PLL (Phase Locked Loop)

4.5.1 Overview Description

The Preshower Control System makes use of the PLL ASIC originally developed for the CMS Tracker Control System. This circuit is a key component in the timing chain, as it receives the specially coded clock and level-1 trigger and regenerates them separately. In addition the **clock output** can be shifted in steps of 1.04 ns over the full 25 ns range by programming an internal register. The **level-1 trigger output** can instead be shifted in multiples of the clock period up to a total of 15 clock cycles. For protection against Single Event Upsets (SEU) due to radiation, the PLL logic is protected by triple voting. The PLL was designed with stringent jitter requirements and low power dissipation. (get measurement values…)

The basic architecture of the PLL is shown in Figure 4.11. The ASIC is essentially composed of the following functional elements: the Trigger Decoder logic, the TPLL & Phase Shifter, the I2C Interface and the Auto-Calibration logic.

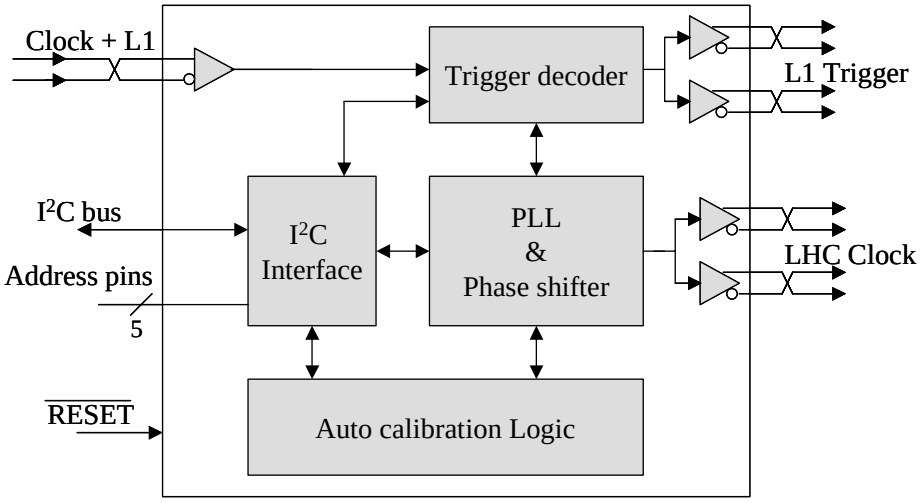


Figure 4.11 Block diagram of the PLL ASIC.

The PLL IC features two clock output buffers and two trigger output buffers for increased driving capability. This feature would be very useful for the Preshower motherboard implementation. All outputs are at standard LVDS levels. The timing of the clk and trigger level signals generated by the PLL ASIC is shown in Figure 4.12. What is the skew between the two clk outputs ?

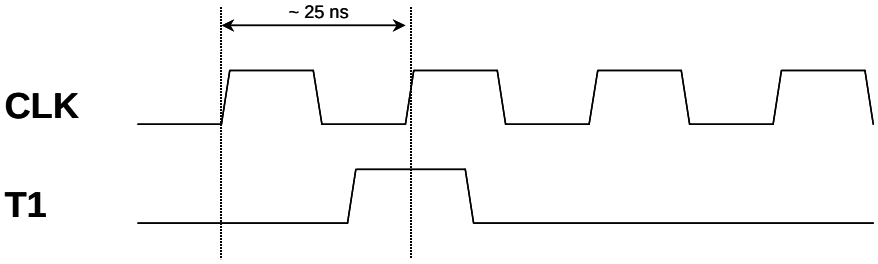


Figure 4.12 Clk and Trigger Level 1 signals from the PLL.

For full details on this circuit, the reader is referred to the "CMS Tracker PLL Reference Manual", Version 2.0, July 2000.

4.5.2 ASIC design status (December 13, 2000)

The IC has been fabricated in the 0.25µm Radiation Tolerant technology. Prototypes are available on request. (Small volume.) Packaging ?

4.6 The DCU (Detector Control Unit)

4.6.1 Overview Description

The (DCU) Detector Control Unit is a mixed signal ASIC dedicated to local measurement of environmental parameters. The functionality of this chip in the Preshower slow control system is not specified yet but the system architecture supports its presence. The DCU is connected to a CCU through an I^2C serial interface. The DCU is acting as a slave device. The Block diagram of the CCU ASIC is shown in Figure 4.13.

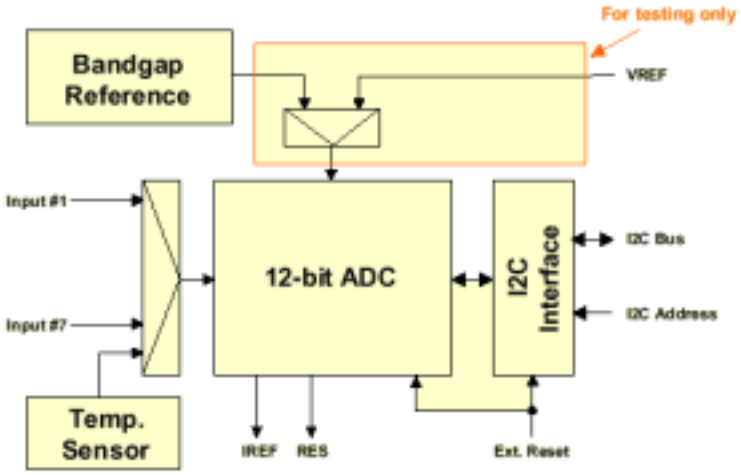


Figure 4.13 Block Diagram of the DCU ASIC.

The core of the DCU is a 12-bit slow analog to digital converter which can be used with the on chip multiplexer to access several sources, such as voltages and currents. One could envisage to monitor detector power supply voltages and/or currents. In addition an on chip band-gap based temperature sensor is foreseen for temperature monitoring without the need of external transducers.

The DCU specifications are summarized in the following table: (***preliminary***)

- Input channels: 7 (5 used) (+ Internal Temperature Sensing)
- Resolution: 12 bits
- INL: ±1 LSB
- DNL: no missing codes
- Conversion time: < 1ms
- Operating temperature range: -50 °C ~ +50 °C
- Power Consumption: < 50 mW
- Supply Voltages: VSS = -1. 25V and VDD = 1. 25V
- Clock Frequency: 40 MHz (in phase with APV clock)
- Input range: GND _ 1.0V
- Die Size: 2 mm x 2 mm

4.6.2 ASIC design status (December 13, 2000)

Under development. No prototype available for distribution.

Documentation ?

Final specs ?

4.7 The TU (Transceiver Unit)

4.7.1 Overview description

Converts the optical signals to electrical and vise versa. Provides the Hardware Reset signal. Needs an I2C connection for programming the Laser driver bias current. After a hardware Reset condition the bias current is set to the maximum facilitating a good transmission. The user can lower the bias current to prolong the life of the laser diode.

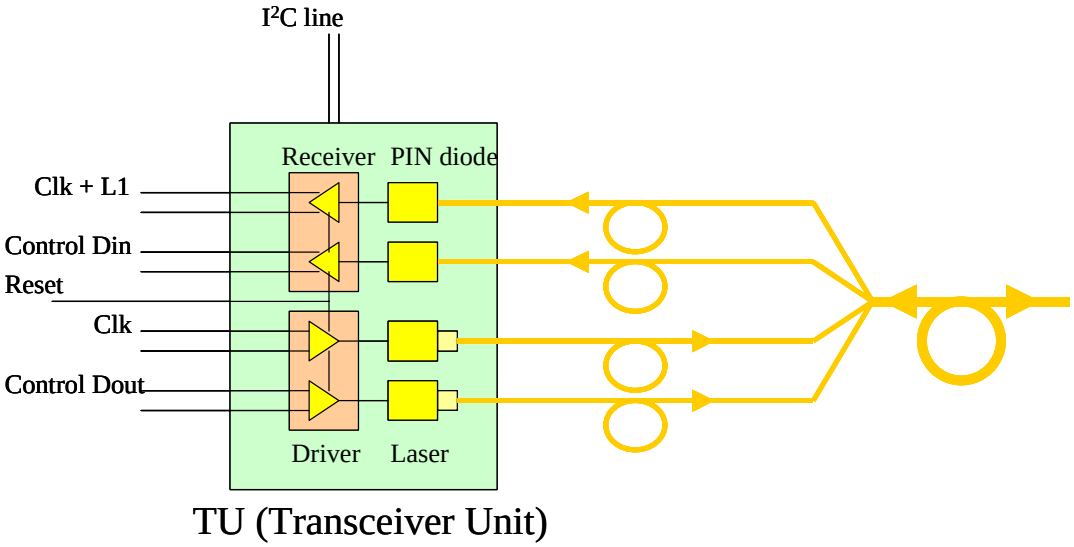


Figure 4.14 Transceiver Unit block diagram.

Implemented on one of the motherboards connected on the same Ring. The Hardware Reset signal has to be relayed on the rest of the motherboards participating on the same Ring.

4.7.1.1 The Laser Diode

A commercial component. InGaAs MQW edge emiting diode,

4.7.1.2 The Laser Driver

A 0.25μ Rad-Tol chip.

4.7.1.3 The Pin Diode

A commercial component InGaAs pin diode. Performance will be affected by radiation but the Optical Receiver preamplifier will compensate for the degradation of the photodiode quantum efficiency.

4.7.1.4 The Optical Receiver

The block diagram of the Optical Receiver chip is shown in Figure 4.15. The front-end element of the chip is a transimpedance amplifier, which amplifies the

photocurrent delivered by the PIN diode and detect the presence of a hardware reset signal.

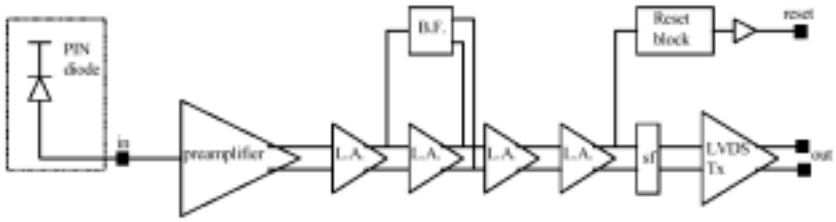


Figure 4.15 Architecture of the Optical Receiver chip.

To allow the distribution of a hardware reset to embedded CCUs, a special extension of the control link transmission protocol allows the generation of a reset at the level of the optical receiver in the embedded electronics. The transmission protocol foresees that the **Hardware Reset** signal is coded as missing pulses on the Data line fiber for long period of time (>2μsec). The Reset block in the Optical receiver will detect the "quiet" state on the Data fiber and respond to it by changing the status of a flag on a dedicated output line generating a reset on the embedded ring. The timing diagram of the Hardware Reset signal generation is shown in Figure 4.16.

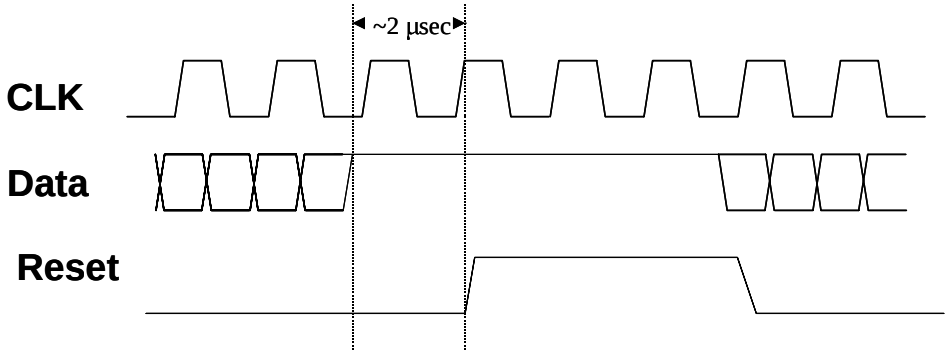


Figure 4.16 Timing diagram of the Reset signal generation.

4.7.1.4.1 Design Status (Dec. 15, 2000)

Prototype on 0.25μ Rad-Tol exists.

4.8 The FEC (Front End Controller)

4.8.1 Overview description

The basic function of the FEC (Front end Controller) module is to interface the Preshower slow control system in the counting room to the embedded control and monitoring electronics on the detector. The FEC module serves as a network controller for the Ring Network that connects the CCU chips sitting on the detector. It handles all the communication between the CCU chips and the counting room electronics and carries out all the Ring Network management tasks.

The block diagram of the FEC module is shown in Figure 4.17. The FEC connects to the Ring Network with two optical ports, the upstream port and the downstream port. It interfaces with the Slow Control Processor through a PCI port. Physically the FEC is implemented as a PMC module and thus can be placed as a piggy-back board on a motherboard (VME board) that hosts the slow control processor. The FEC will primarily interact with the experiments slow control using an appropriate network protocol as defined by the general CMS slow control system.

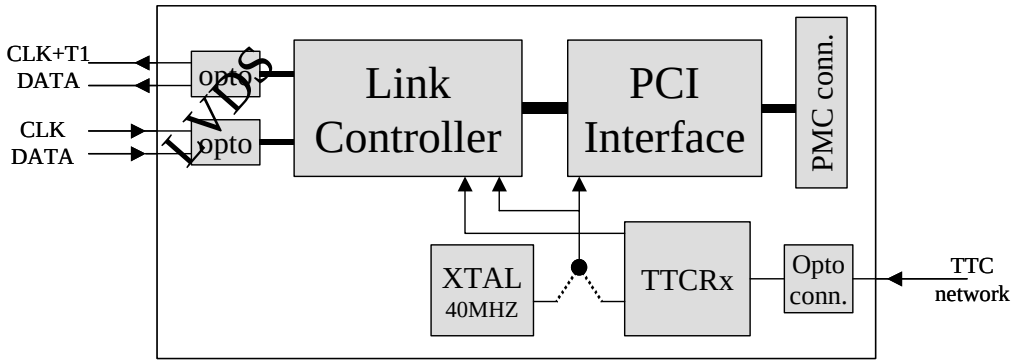


Figure 4.17 Block Diagram of the Front End Control module.

The FEC has an optical input port to receive fast timing information from the TTC distribution network. It is equipped with a TTCrx module which is used to generate the clock for the Ring Network as well as to insert Trigger Commands (and other fast timing signals like the BC0 ??) in the upstream network fiber. When no TTC network connection is present, an on-board crystal oscillator (XTAL) at 40MHz can be used on the FEC. In this mode of operation Trigger commands cannot be issued to the FE chips.

For more information on this module the reader is referred to the "FEC, Front End Control Unit for Embedded Slow Control", C. Ljuslin, C. Palliard, Draft).

4.8.2 Design Status (December 15, 2000)

The current prototype PMC module has LVDS ports for the Ring network. Currently the redundancy schema is not supported. 

5 System Integration

5.1 General Front End System Layout

5.1.1 Electrical Levels on FE chip Interfaces

5.2 Micromodule

The *micromodule* is composed of three elements: the silicon detector and the readout hybrid. The readout hybrid is a printed circuit board that holds the PACE chipset and the DCU chip. A block diagram of a micromodule is shown in Figure 5.1.

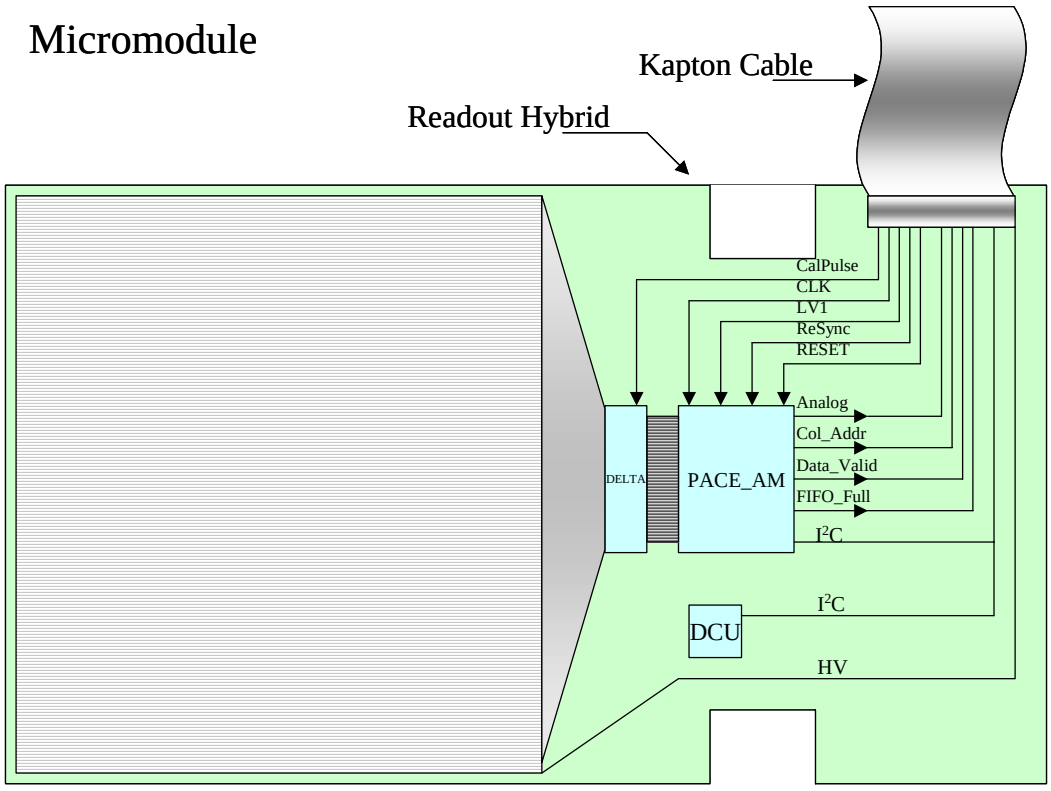


Figure 5.1 A Micromodule with its elements.

The kapton cable connecting the readout hybrid to the motherboard is soldered on the Readout hybrid side and has a connector at the other end to connect to the motherboard. Table 5.1 lists the kapton cable connections and gives a short description for each one. The total number of circuits on the kapton cable has to be accommodated in the small available space foreseen for the cable placement on the micromodule. It should also be taken into consideration for choosing the appropriate connector for the motherboard.

Table 5.1 Kapton Cable signals.

Name	# of wires	Level	Description
Cal_Pulse	2	LVDS	Calibration Pulse
PACE_Clk	2	LVDS	Sampling Clock, 40MHz
ReSync	2	LVDS	Pipeline & Sequencer Reset
LV1	2	LVDS	Level 1 Trigger
Reset	1	CMOS 5V	Resets all state machines
Col_Addr	1	CMOS 5V	Serial Column Address output
Data_Valid	1	CMOS 5V	Data Qualifier signal
FIFO_full	1	CMOS 5V	Pipeline Overrun Flag
I^2C	2	Open col.	Slow Control port
Analog	1	analog	PACE analog output
5V_AGND	1	power	5Volt Analog Power (PACE)
5V_AVDD	1	power	
5V_DGND	1	power	5Volt Digital Power (PACE)
5V_DVDD	1	power	
2.5V_DGND	1	power	2.5Volt Digital Power (DCU)
2.5V_DVDD	1	power	
HV	1	power	Detector High Voltage
GND	1	power	
TOTAL =	**23**		

5.3 Motherboard

The *motherboard* contains the electronics necessary to digitize and transmit the signals from the very front-end chip PACE situated on the micromodules. It also receives, regulates and distributes the power to the Front-End electronics. A typical block diagram of a motherboard is shown in Figure 5.2.

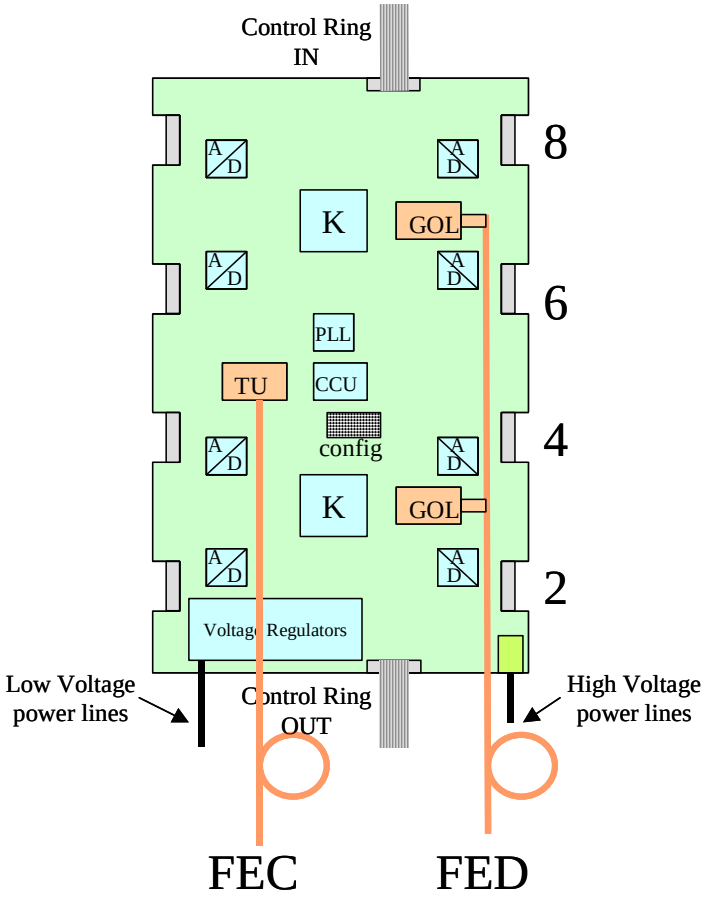


Figure 5.2 Block Diagram of a motherboard.

The major electronic elements installed on a motherboard are:

- a number of ADCs, one for each micromodule on the same the motherboard,
- a number of K-chips, one for every 4 ADCs,
- one CCU chip,
- one PLL chip,
- a number of GOL chips, one for every K-chip,
- a number of LASER diode transmitters, one for every GOL chip,
- one TU, installed only on master control type motherboards (see below),
- a series of regulators for the different low voltage power supply levels. The necessary power supply voltages are listed bellow:
    - 5V (PACEs analog power supply),
    - 5V (PACEs digital power supply),

- 5V (ADCs analog power supply),
- 5V (ADCs digital power supply),
- 2.5V (K-chip, CCU, PLL, DCU, GOL, TU) (two regulators might be needed if the current rating for one regulator is exceeded.).

The motherboard attaches to the system through the following connections:

- Optical:
  - Readout Link (Bundle of cables)
  - Control Link (Bundle of cables)
- Electrical:
  - Control Ring loop (2 ports)
  - Power supply lines (Low Voltage, High Voltage)

5.3.1 Motherboard Types

To entirely cover the Preshower endcap disk with sensors it is necessary to have four different types of motherboards with different shapes, as shown in Figure 5.3. These motherboard types can accommodate different number of micromodules varying between 7 to 10, as shown in the figure.

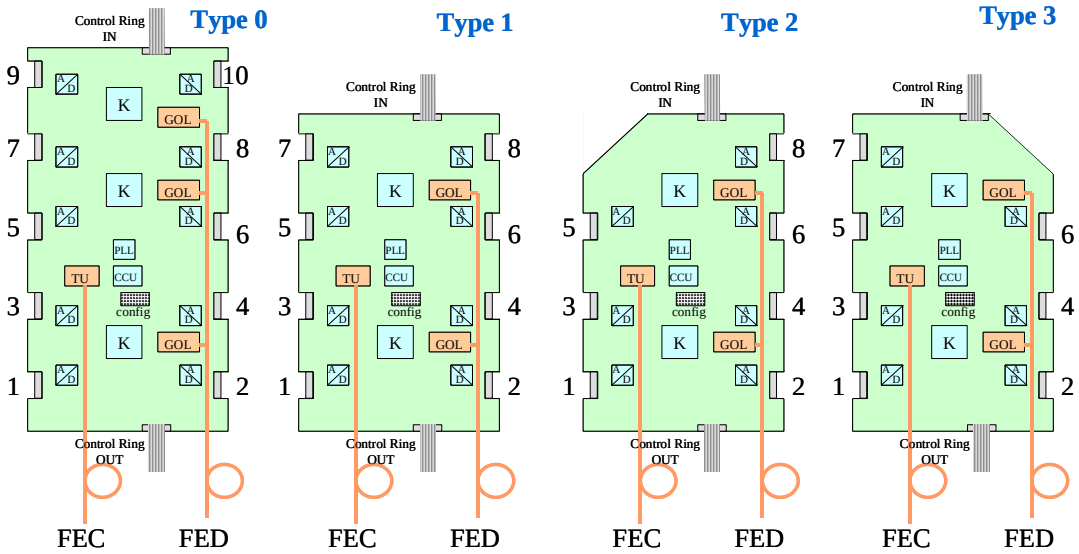


Figure 5.3 The four motherboard types.

5.3.2 Control Rings

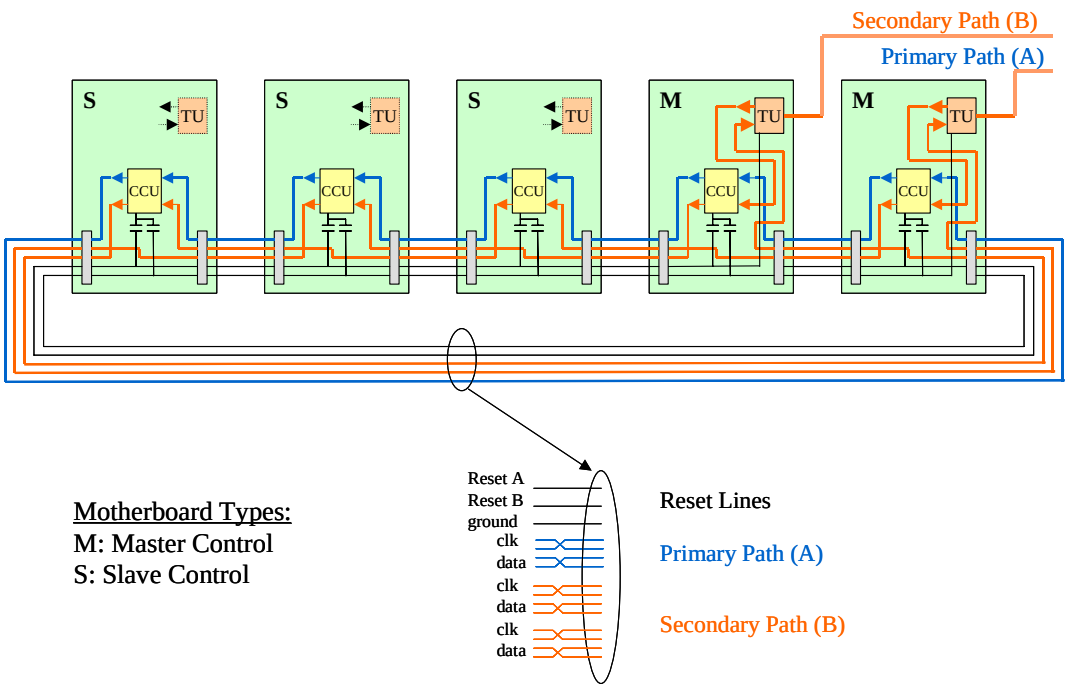


Figure 5.4 Redundancy scheme on the Control Rings.

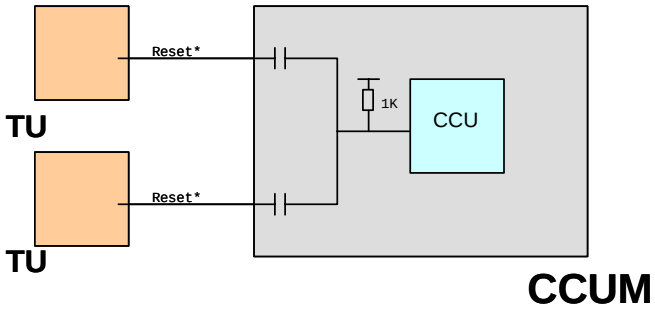


Figure 5.5 Or-ing the Reset signal from two Transceiver Units.

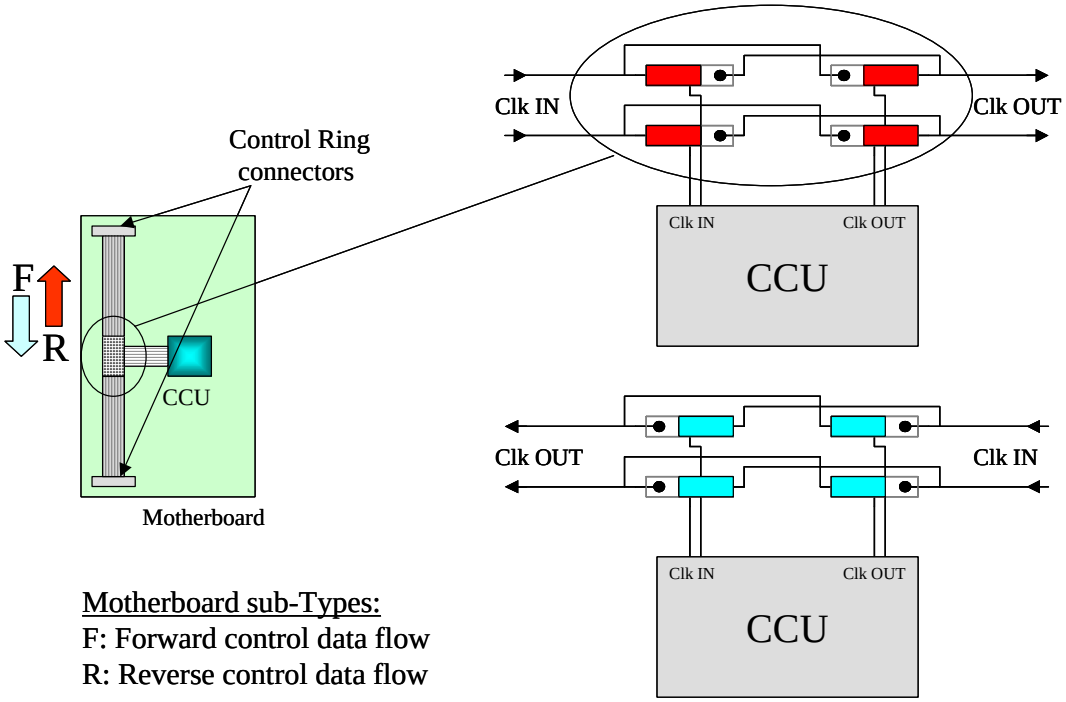


Figure 5.6 Direction of the Control Data flow on the motherboard.

5.3.3 Motherboard numbering schema

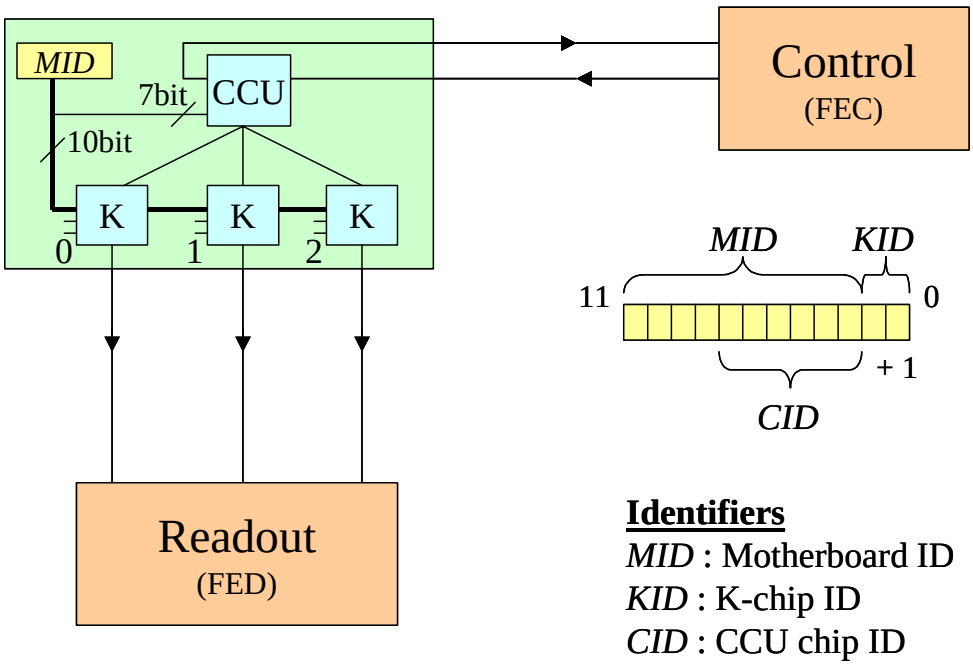


Figure 5.7 Motherboard ID assignment.

5.4 Detector Partitioning

5.4.1 Readout Links

5.4.2 Control Links

6 Power Distribution

Control and monitoring of power distribution on the Front End electronics.

6.1 Low Voltage

6.2 High Voltage

7 Appendixes