CMS Electronics Week
May 2001

PRESHOWER Front-End Electronics
Digital Part

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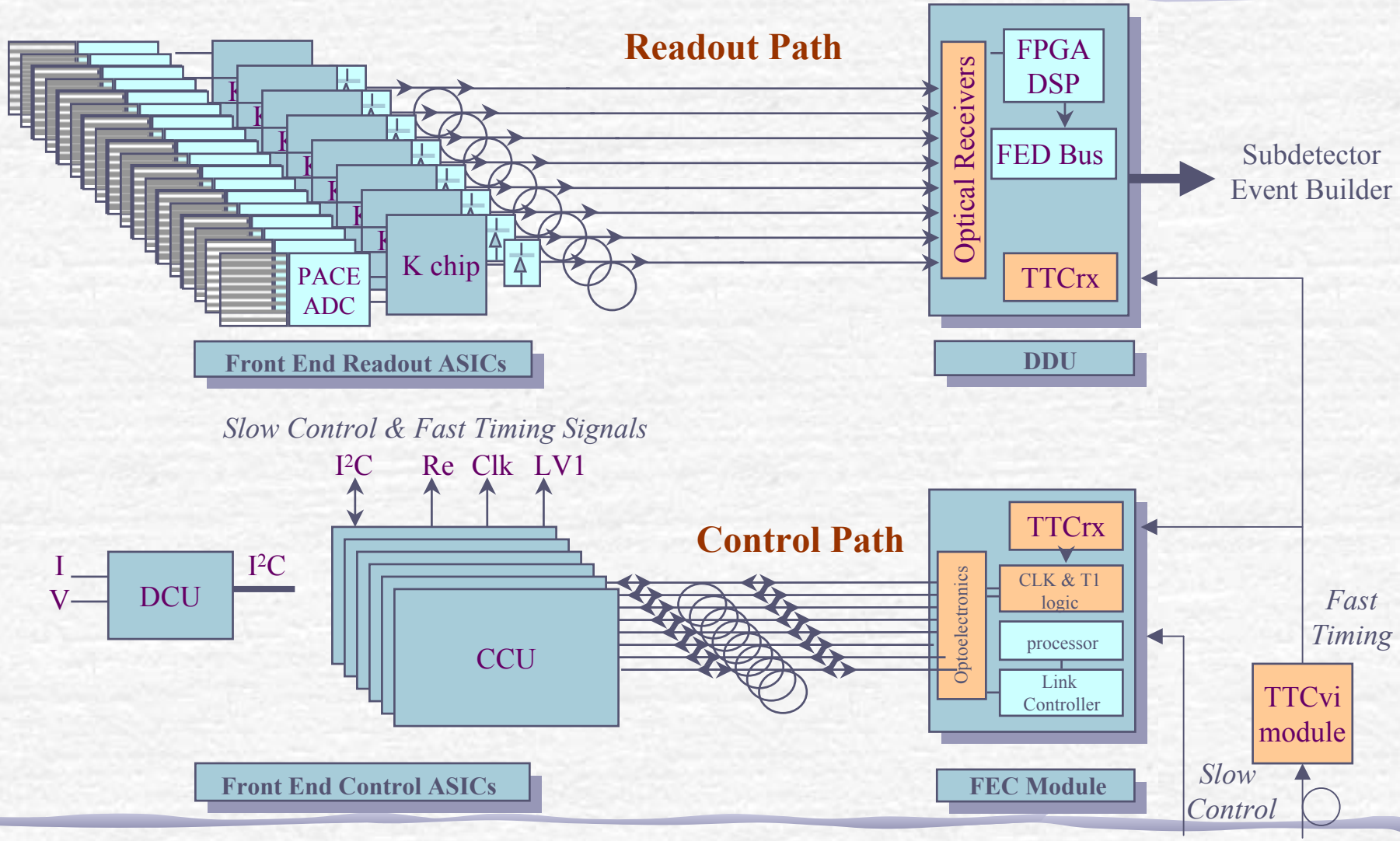
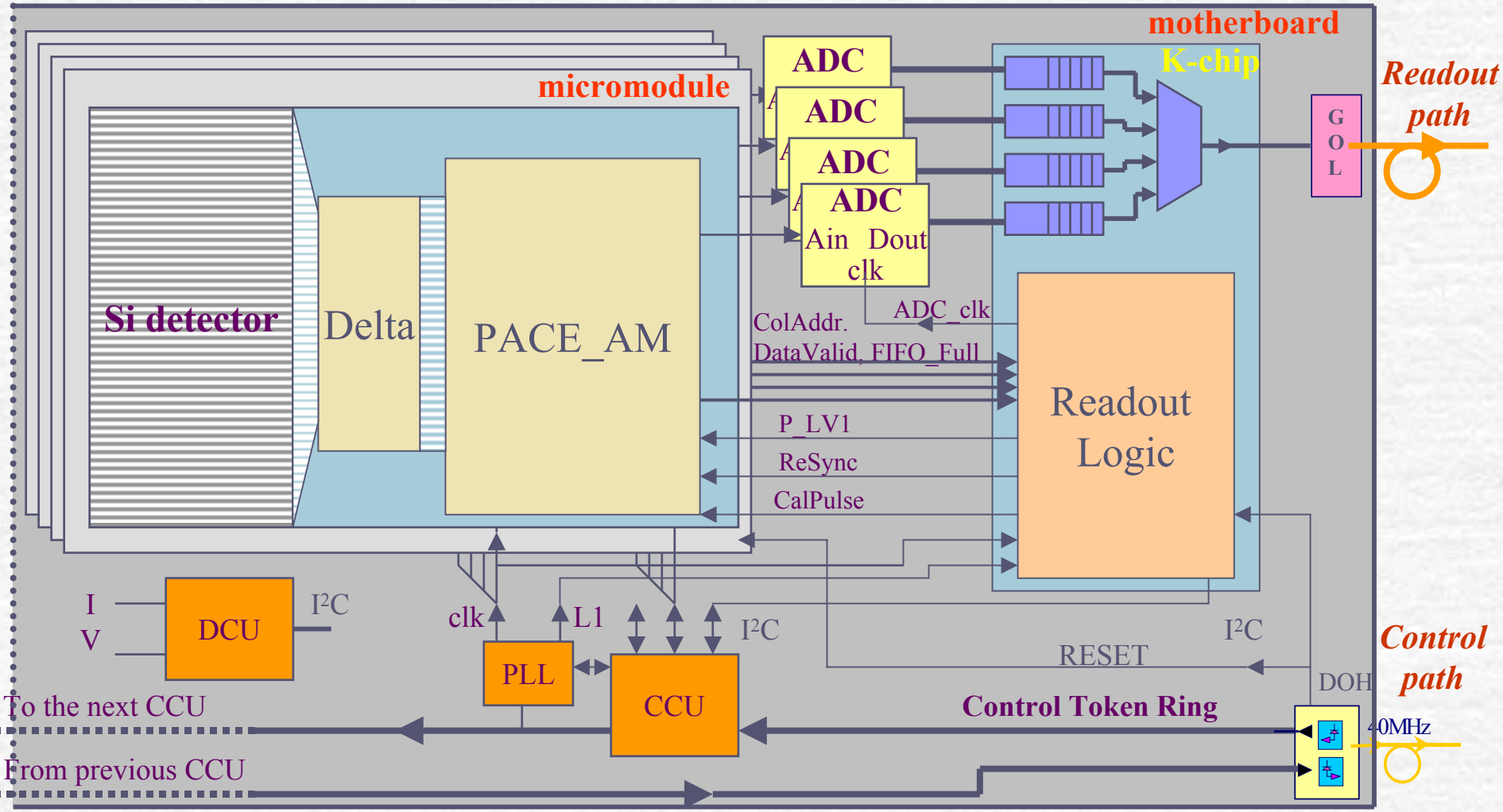
General Readout & Control Architecture



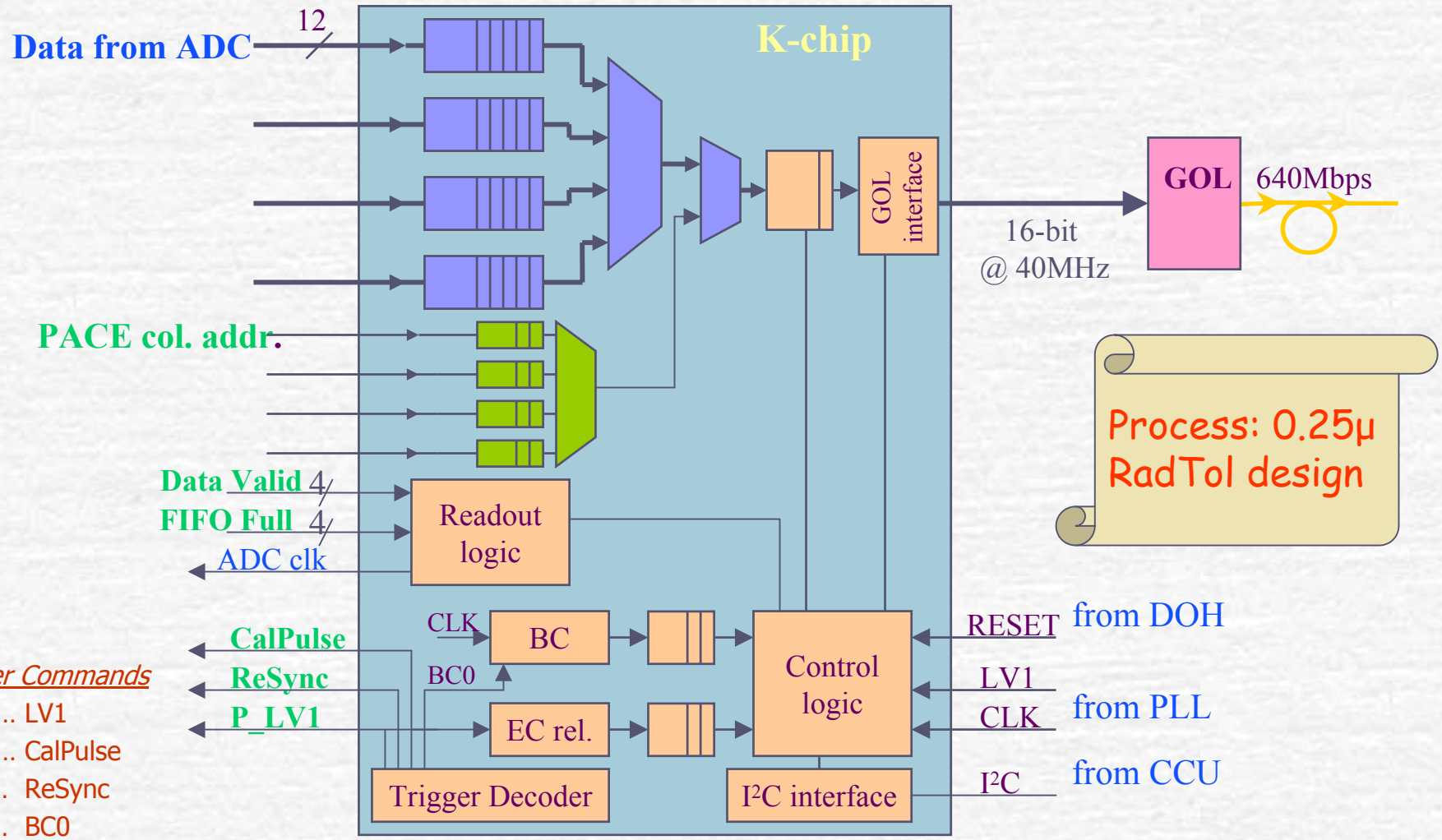
Preshower Readout & Control Front-End Electronics



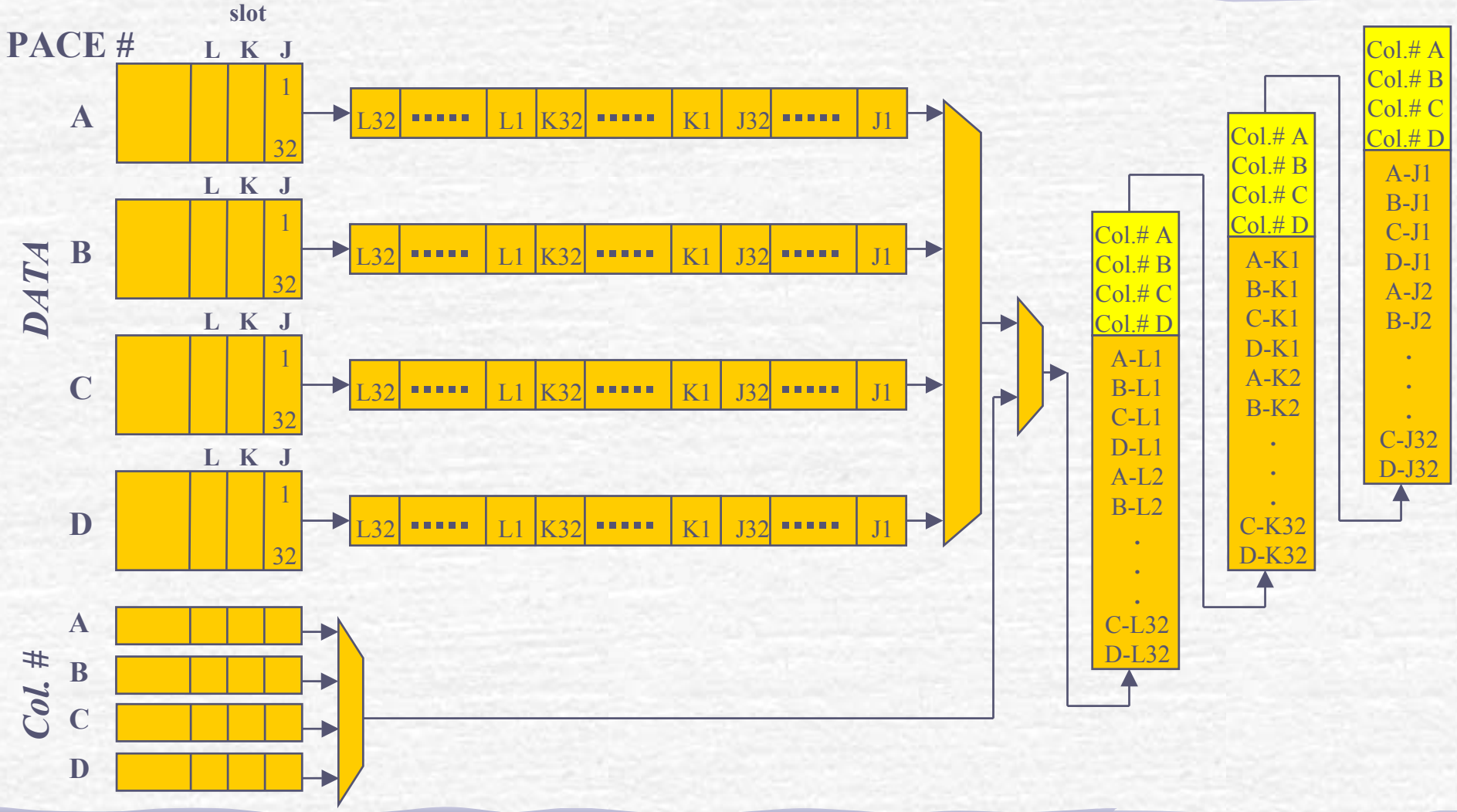
K-chip Functionality

- PACE Readout Control
  - Data concentration from up to 4 PACE chips
  - Masking of the unused inputs
  - No Zero Suppression
  - Bunch Crossing Identification
  - Buffer Overflow Detection / Prevention
- Trigger Decoder Logic
- ADC clock Generation
- Event Data Formatting
  - Data alignment into 16-bit words
  - Null Event Insertion
- Gigabit Optical Link Controller

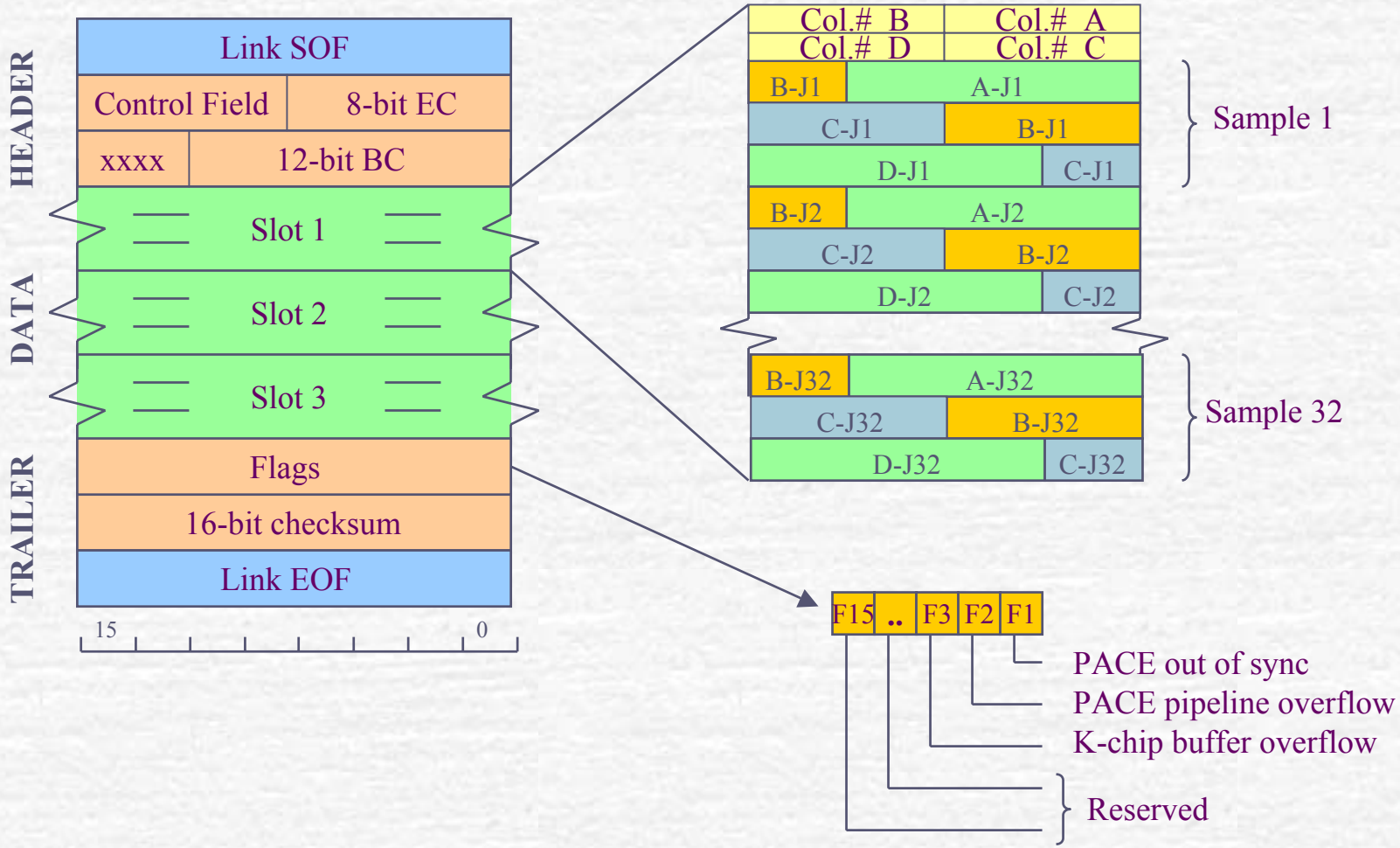
K-chip Block Diagram



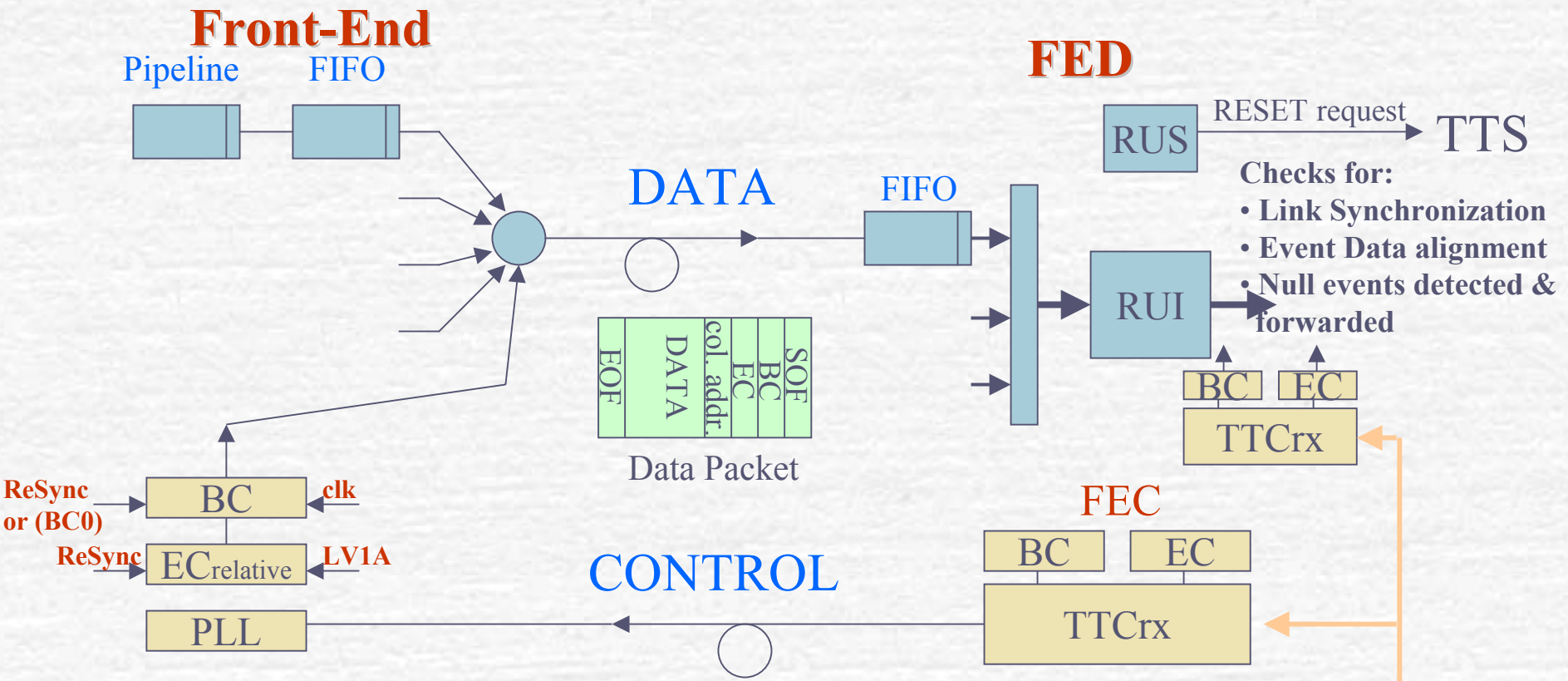
K-chip Data Formatting



Data Packet Format



Readout Synchronization



The K-chip can be programmed to send all or some of the following info:

- BC counter to check for clock line miss/bounce pulses
- $EC_{relative}$ counter to check for LV1A line miss/bounce pulses
- PACE col. addr. for pipeline (PACE) synchronization monitoring

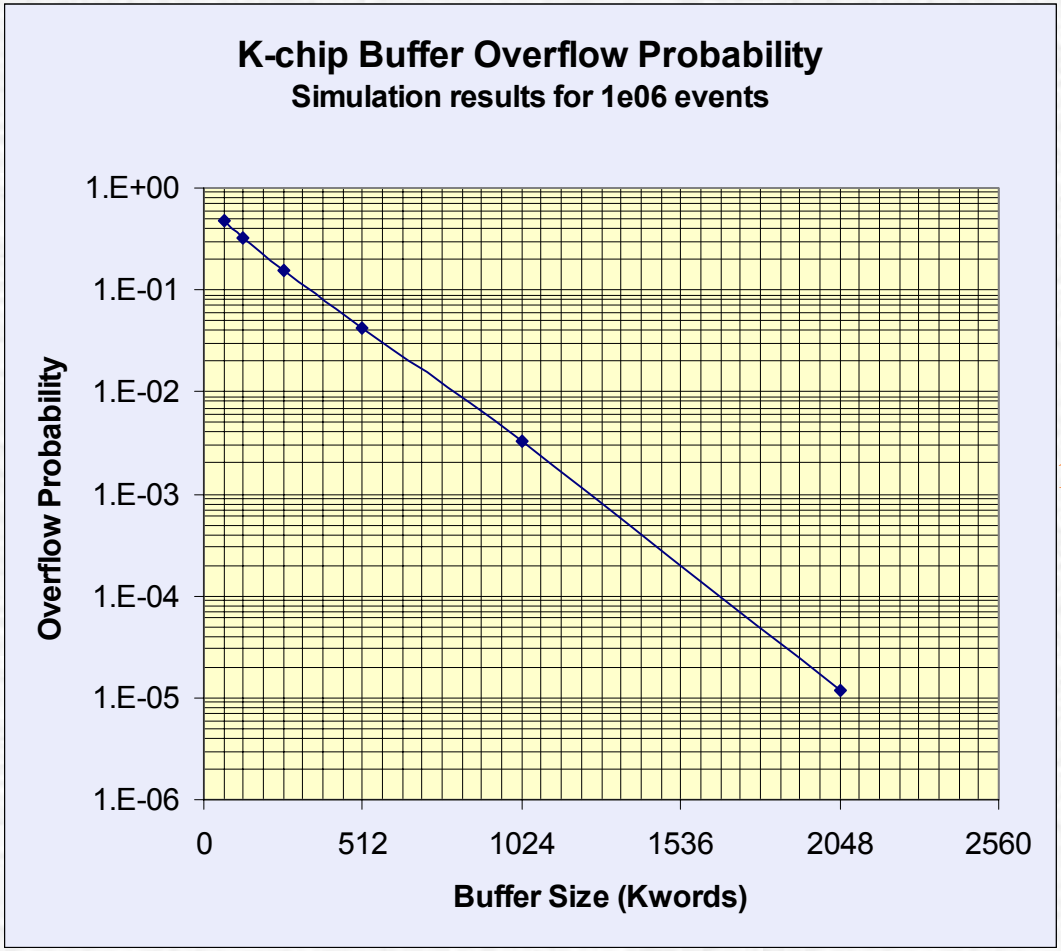
Buffer Overflow

- There are two buffers in the Preshower Front End electronics that are prone to overflow conditions:
  - The Front-End PIPELINE memory (PACE chip)
  - The Front-End Readout FIFO (K-chip)
- The Front End emulator logic in the TCS will protect the Front End chips (PACE & K-chip) from exhibiting overflow conditions.
- Nevertheless, SEU on the Front End logic and spurious or missing Trigger pulses on the fast timing distribution system may cause Front End buffers to overflow.
- K-chip can detect imminent overflow conditions and prevent buffers from actually overflowing and lose synchronization.

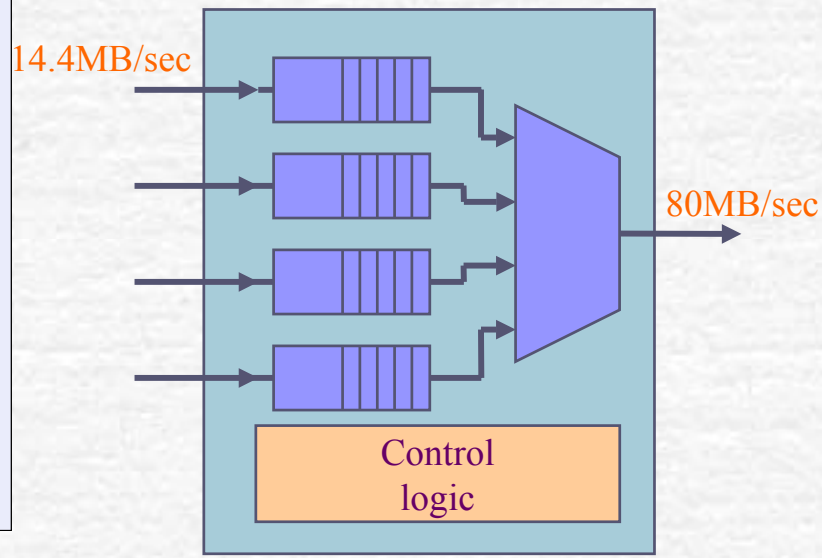
Buffer Overflow Handling

- Front-End PIPELINE memory (PACE chip)
  - PACE Trigger Inhibit Logic on the Front-End (K-chip).
    - If PACE signals an almost full condition then the P_LV1 signal will be gated until some data has been read out and space is made available in the pipeline memory.
    - The readout chain gets informed about the PACE trigger gating condition and null events are inserted to maintain Readout Synchronization. (According to TRIDAS recommendations.)
- Front-End Readout FIFO (K-chip)
  - Readout FIFO will be sized for lower overflow probability than the Pipeline memory.
  - PACE Readout Blocking Logic
    - K-chip discards the event being pushed in by the PACE chips
    - K-chip Event Counter is incremented and
    - A null event is transmitted.
- The PACE Trigger Inhibit logic can be enabled or disabled via I^2C commands.

K-chip Buffer Size



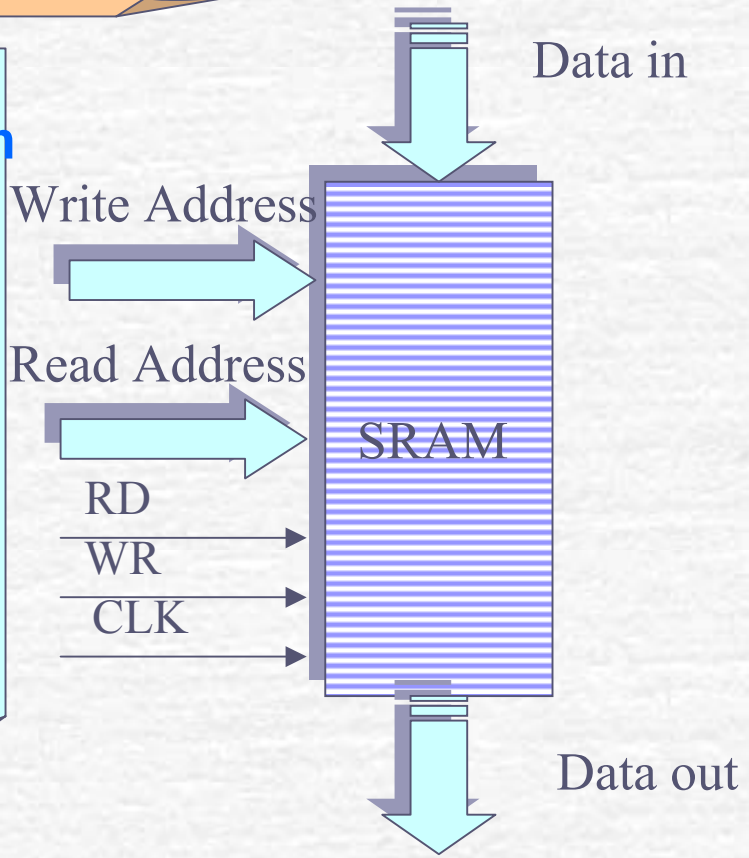
- Samples per Event: 3
- Channels MUXed in: 32
- Trigger Rate: 100KHz
- Link Throughput: 640Mbps



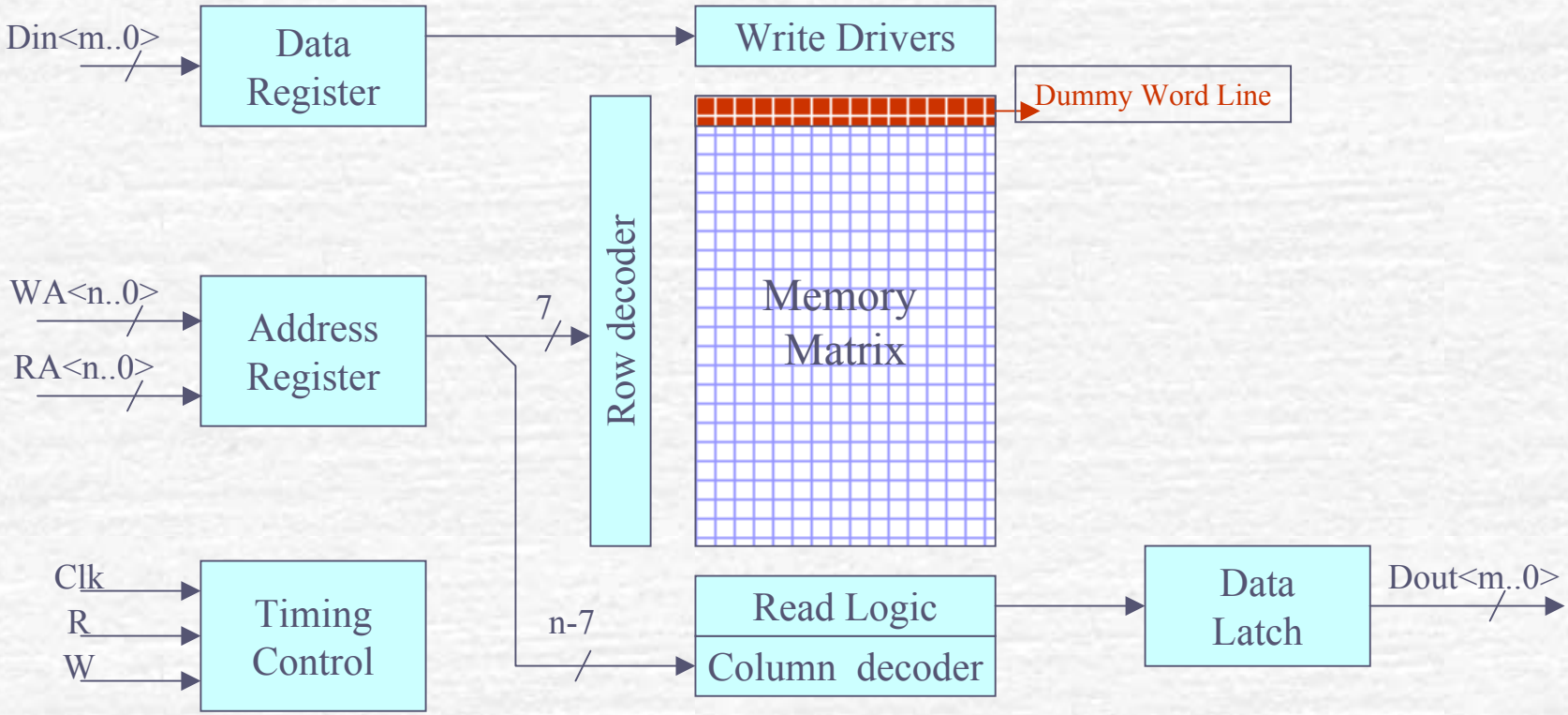
SRAM Features

Rational: No SRAM macro cell existed in RadTol 0.25μ process

- Synchronous *pseudo* Dual Port Operation
- Self timed logic
- Registered Inputs, Latched outputs
- Radiation Tolerant Design
- Typical Operation freq.: 40MHz
- Configurable Macro design
- Data bus width: (n x 9)bits
- Data arrangement: 8 + 1 parity
- Memory Size: up to 4K words



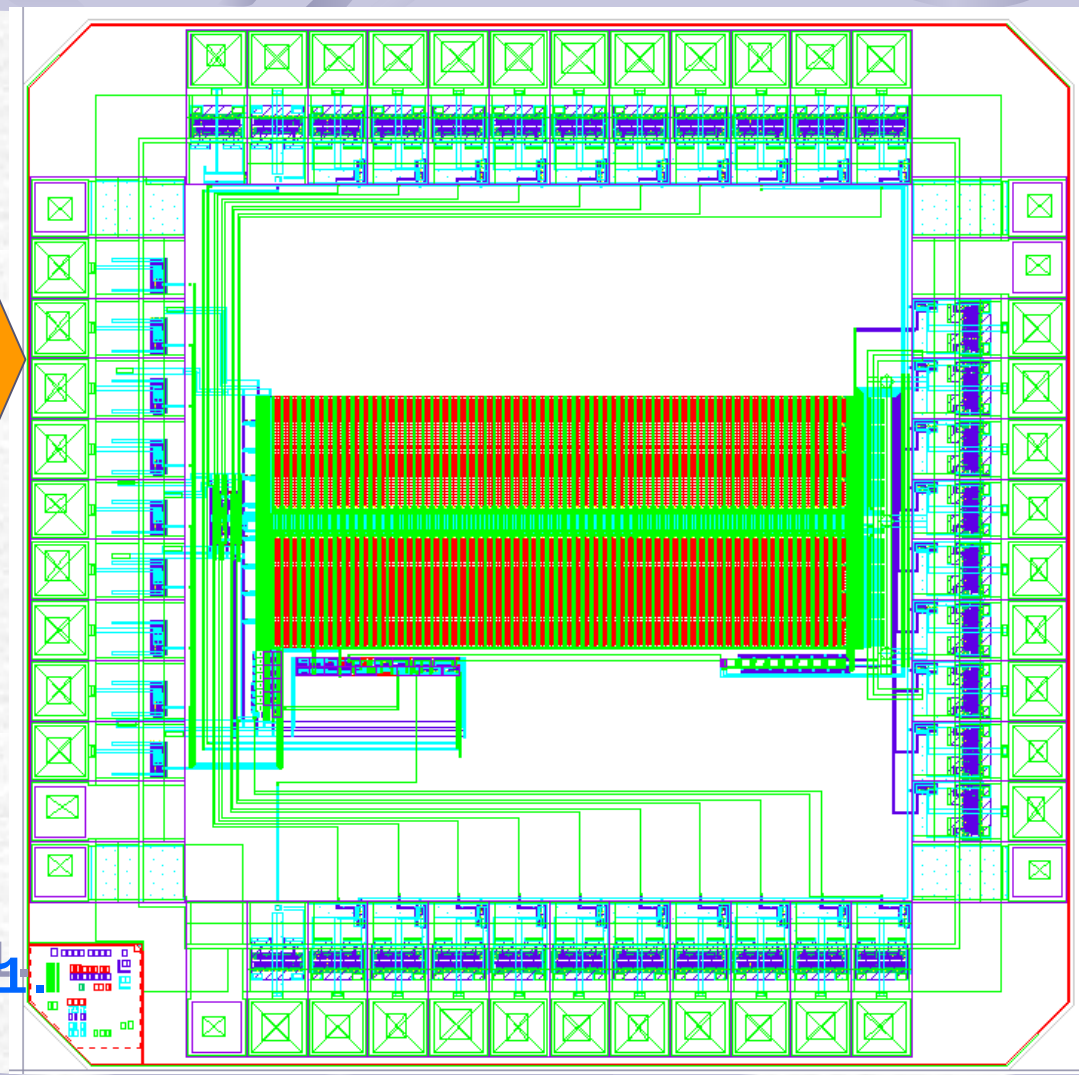
Dual Port SRAM
block diagram



Submitted SRAM Chips

- 1st Prototype (CERN MPW)
- Configuration: 1Kx9 bit
- Size: ~560μm x 1,300μm
- Area: ~0.73mm²
- Submitted: Oct. 2000.
- Chip Received: Feb 2001
- Tested O.K.

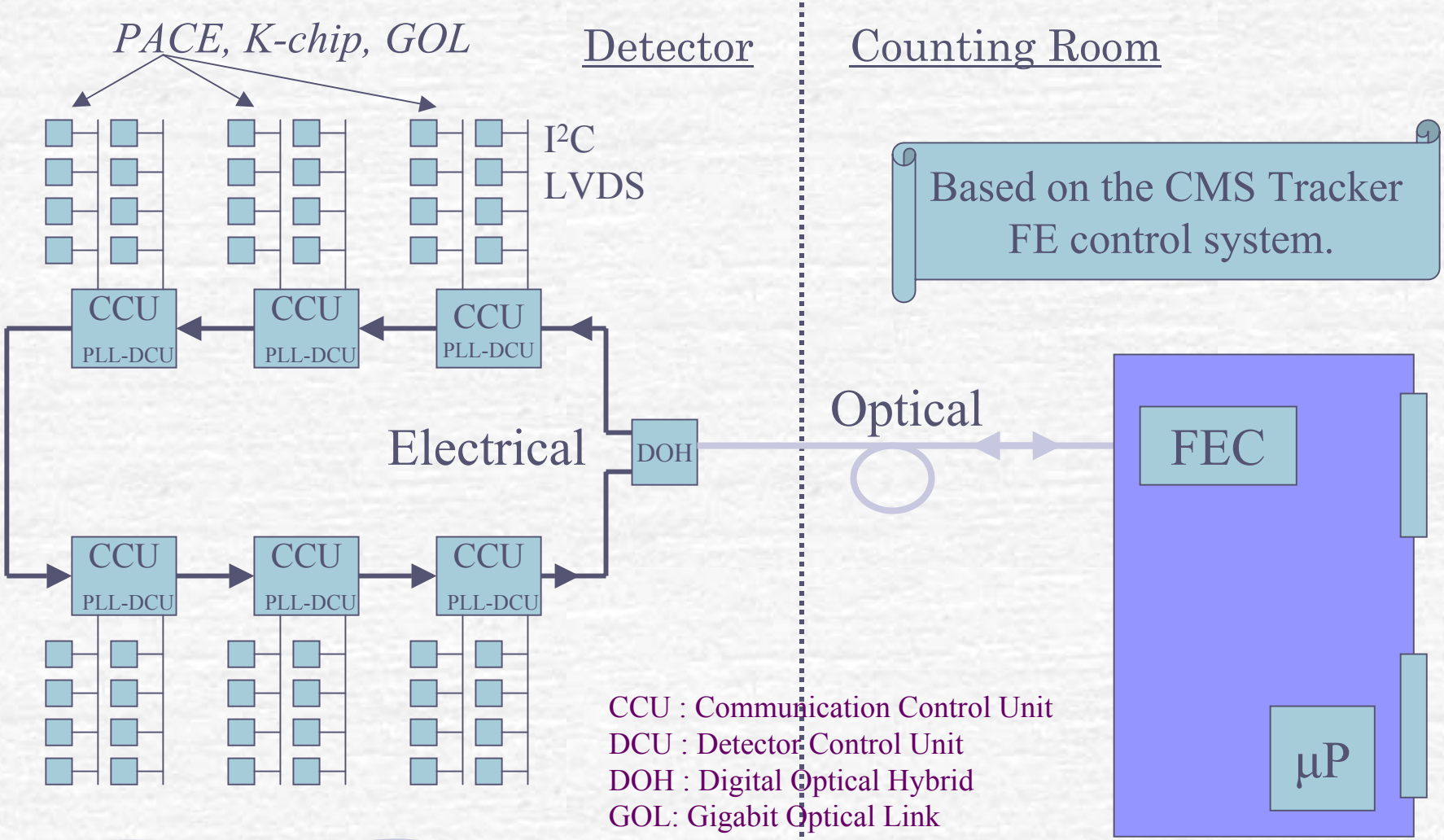
- 2nd Prototype (CERN MPW)
- Configuration: 4Kx9 bit
- Size: ~1,850μm x 1,300μm
- Area: ~2.4mm²
- To be Submitted: May 2001.



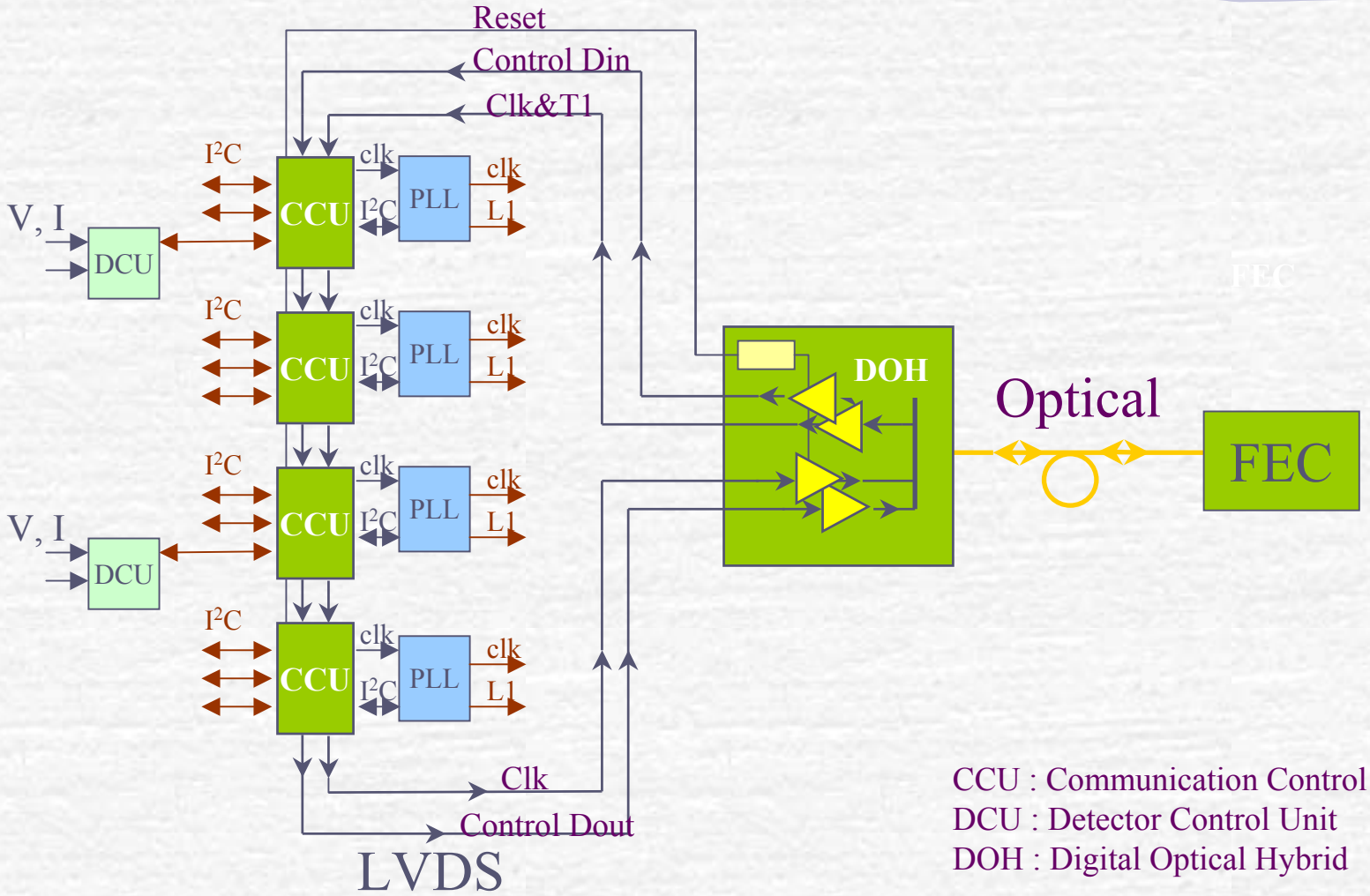
Front-End Control System

- The tasks of the Preshower Front-End Control System are to distribute to the detector embedded electronics:
  - Fast Synchronizing signals and timing information (LHC clock, LV1 trigger, ReSync, BC0) and
  - Slow control information for controlling the status of the detector, monitoring environmental parameters, front-end electronics set-up and calibration and downloading operating condition parameters.
- A derivative of the CMS Tracker control system reusing the ASIC and optoelectronic components developed for the Tracker control system.

Control System Overview

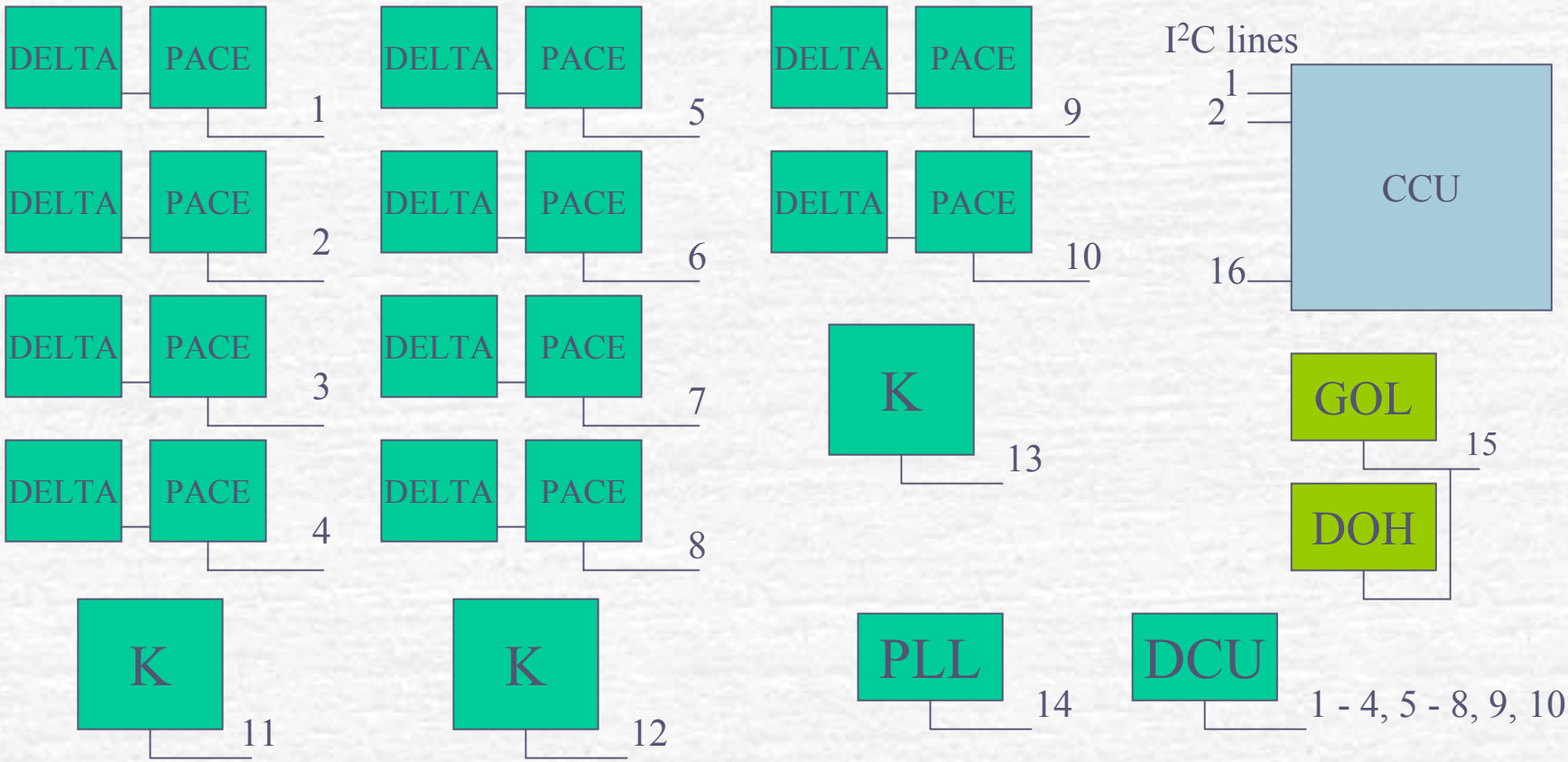


Preshower Control System

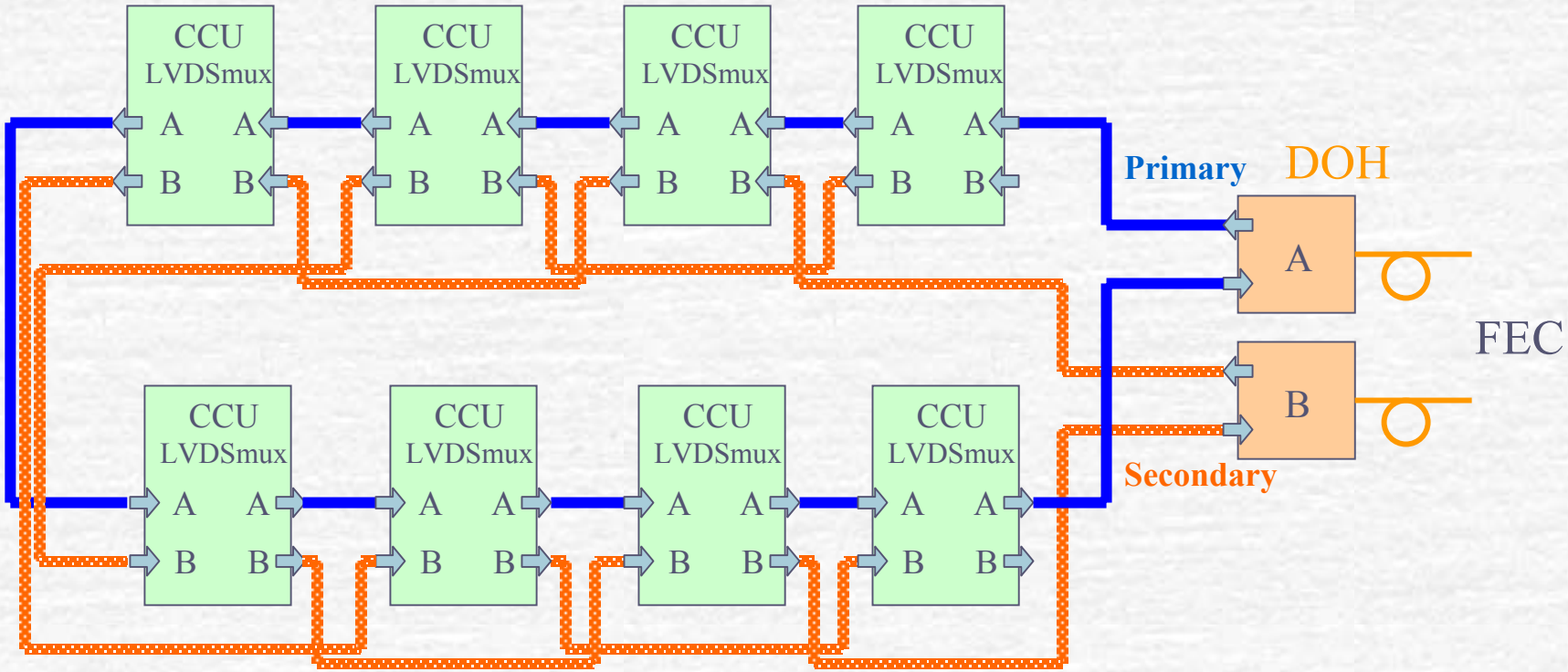


CCU : Communication Control Unit
DCU : Detector Control Unit
DOH : Digital Optical Hybrid

I²C bus distribution

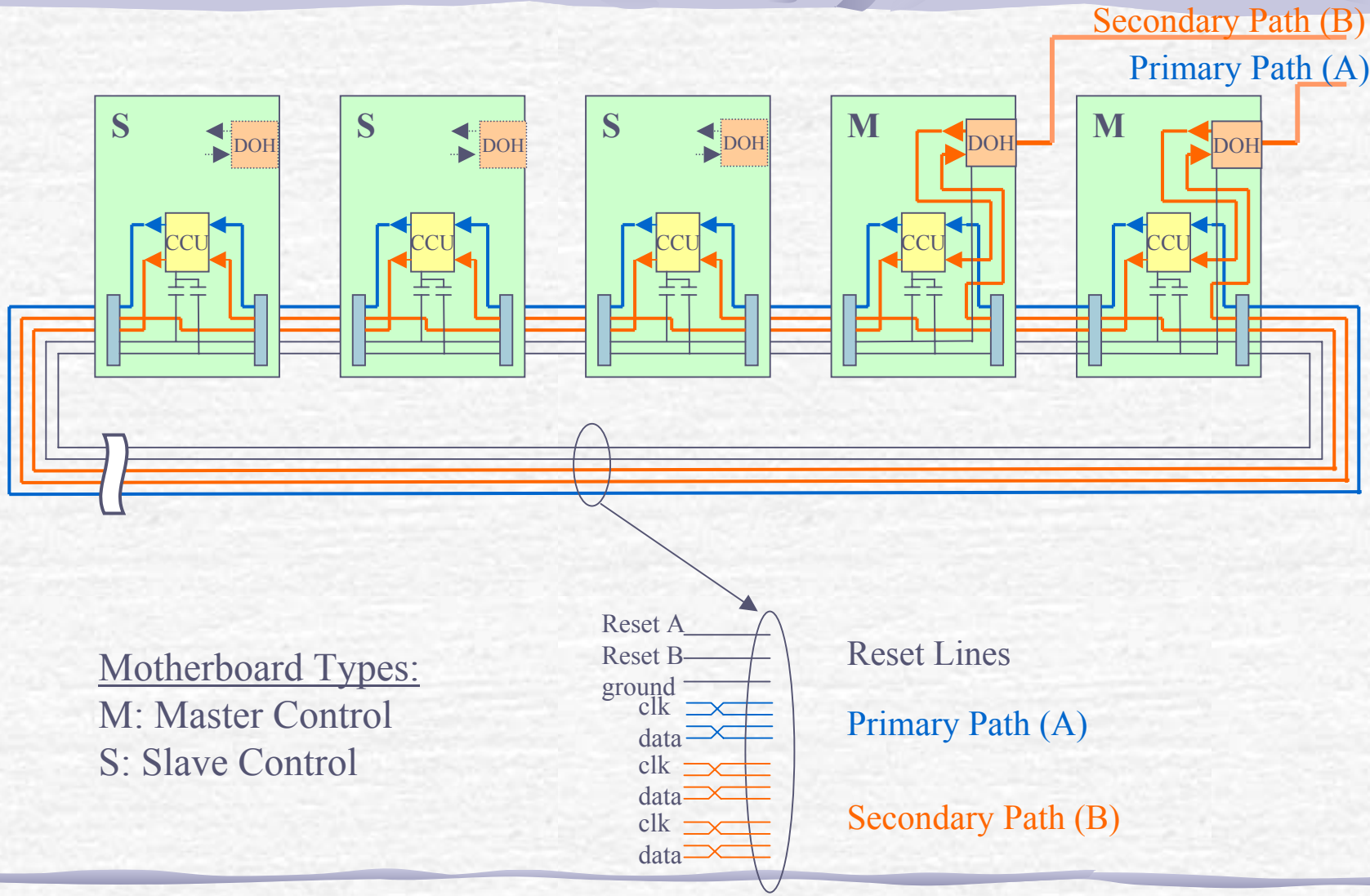


Control System Redundancy



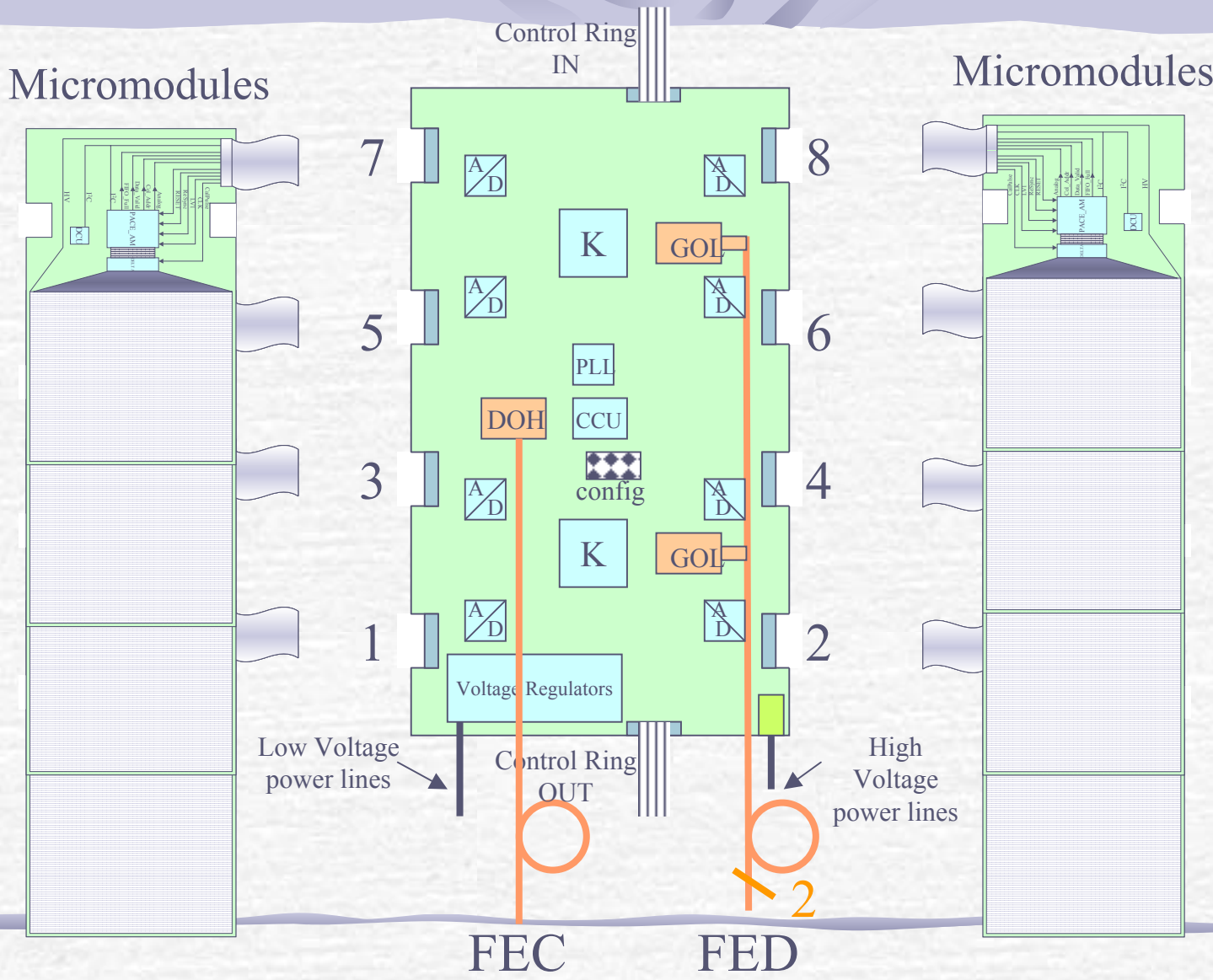
- The primary port A is the default port and is used in normal operation.
- The secondary port B is the auxiliary port and is used when there is a need to bypass a failing CCU chip or a DOH unit on the ring.

Redundancy Implementation

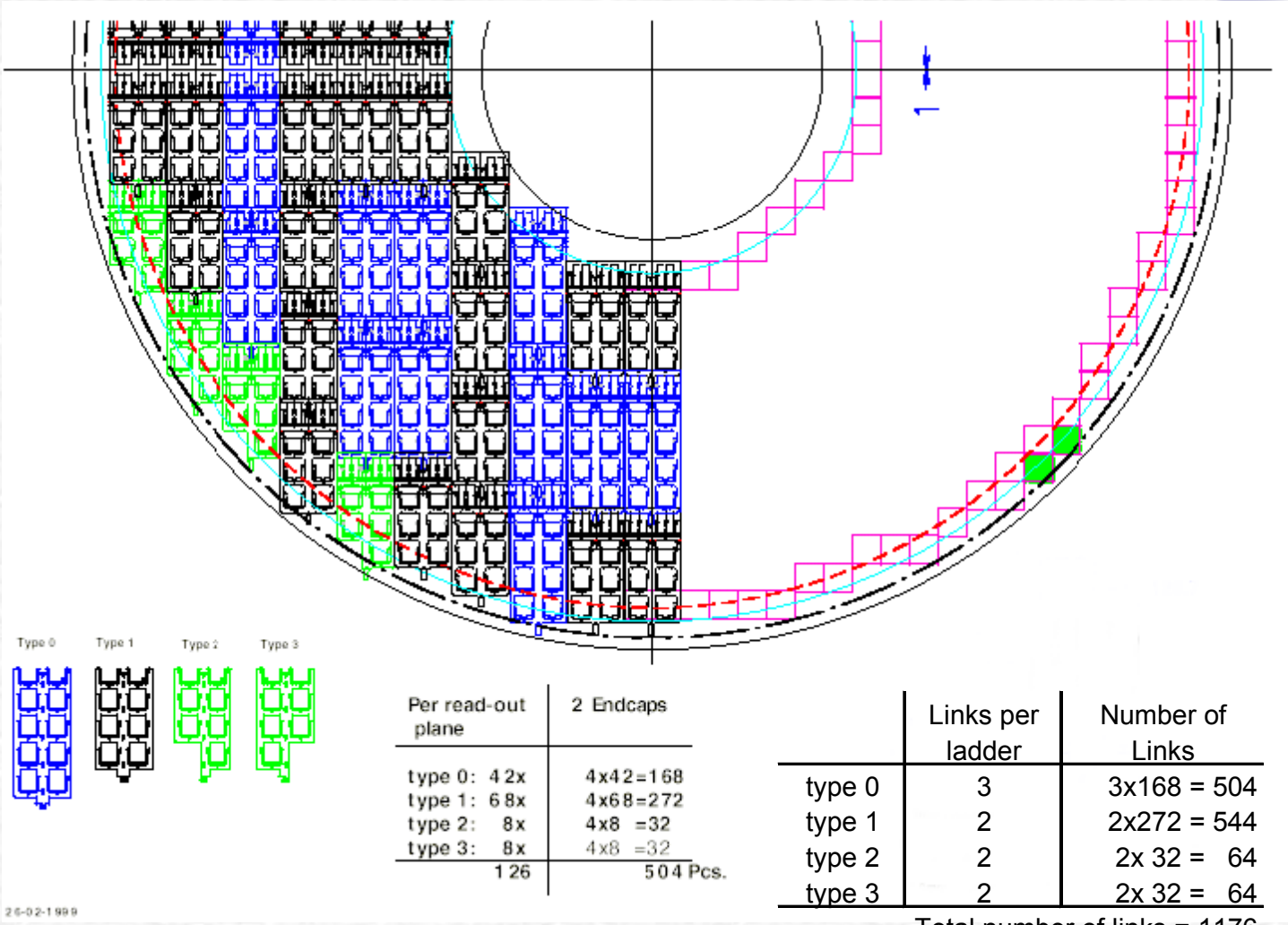


Motherboard Types:
M: Master Control
S: Slave Control

Motherboard



Preshower Endcap

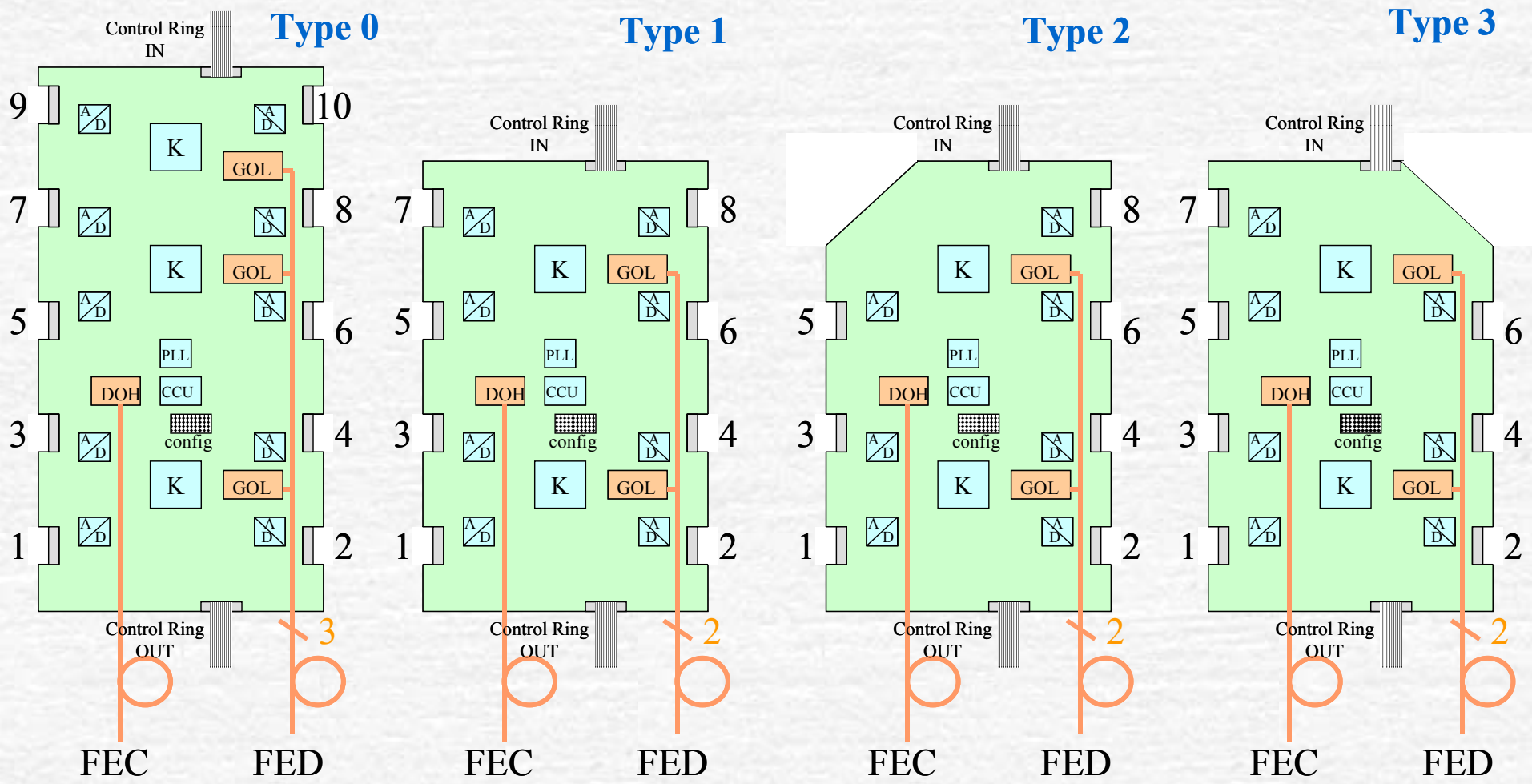


Per read-out plane	2 Endcaps
type 0: 42x	4x42=168
type 1: 68x	4x68=272
type 2: 8x	4x8 =32
type 3: 8x	4x8 =32
126	504 Pcs.

	Links per ladder	Number of Links
type 0	3	3x168 = 504
type 1	2	2x272 = 544
type 2	2	2x 32 = 64
type 3	2	2x 32 = 64

Total number of links = 1176

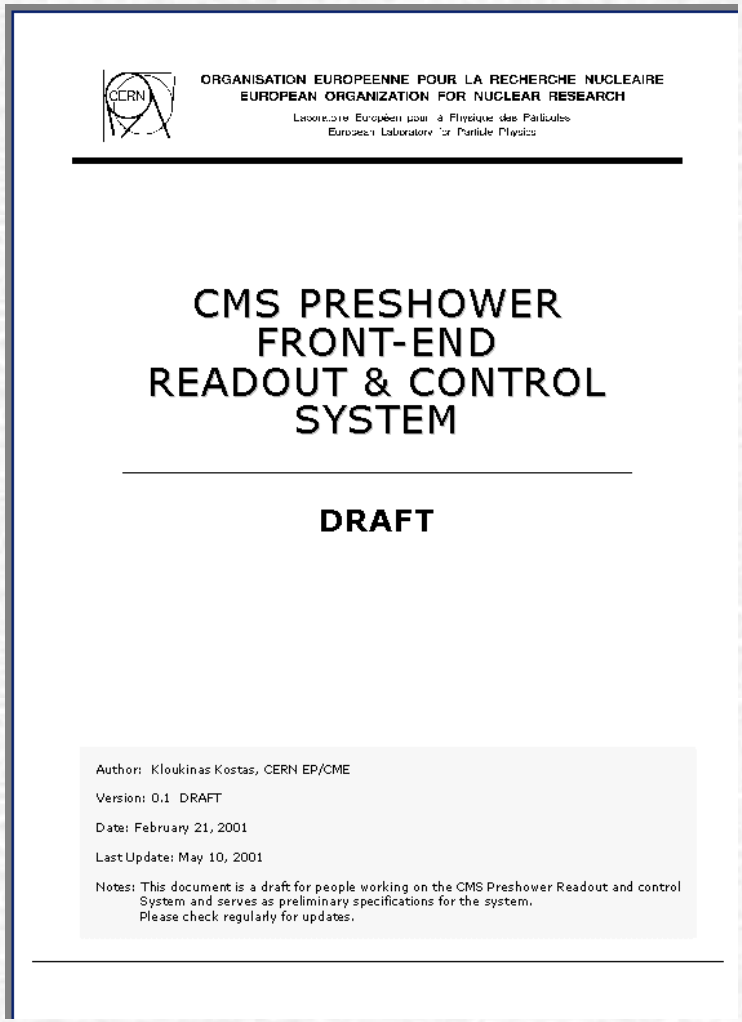
Motherboard Types



Planning

- SRAM
  - Testing of the 2nd prototype expected in Aug. 2001.
- K-chip
  - Expect to submit a 1st prototype in a CERN MPW run around Nov. 2001.
- Motherboard
  - A reduced version, the "K_motherboard", is scheduled to be ready in the beginning of 2002. (A test vehicle for the K-chip readout. This version will not incorporate the "CCU" slow control system.)
  - A first prototype of a full version is planned to be ready in Aug. 2002.

Documentation



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Laboratoire Européen pour la Physique des Particules
European Laboratory for Particle Physics

CMS PRESHOWER
FRONT-END
READOUT & CONTROL
SYSTEM

DRAFT

Author: Kloukinas Kostas, CERN EP/CME

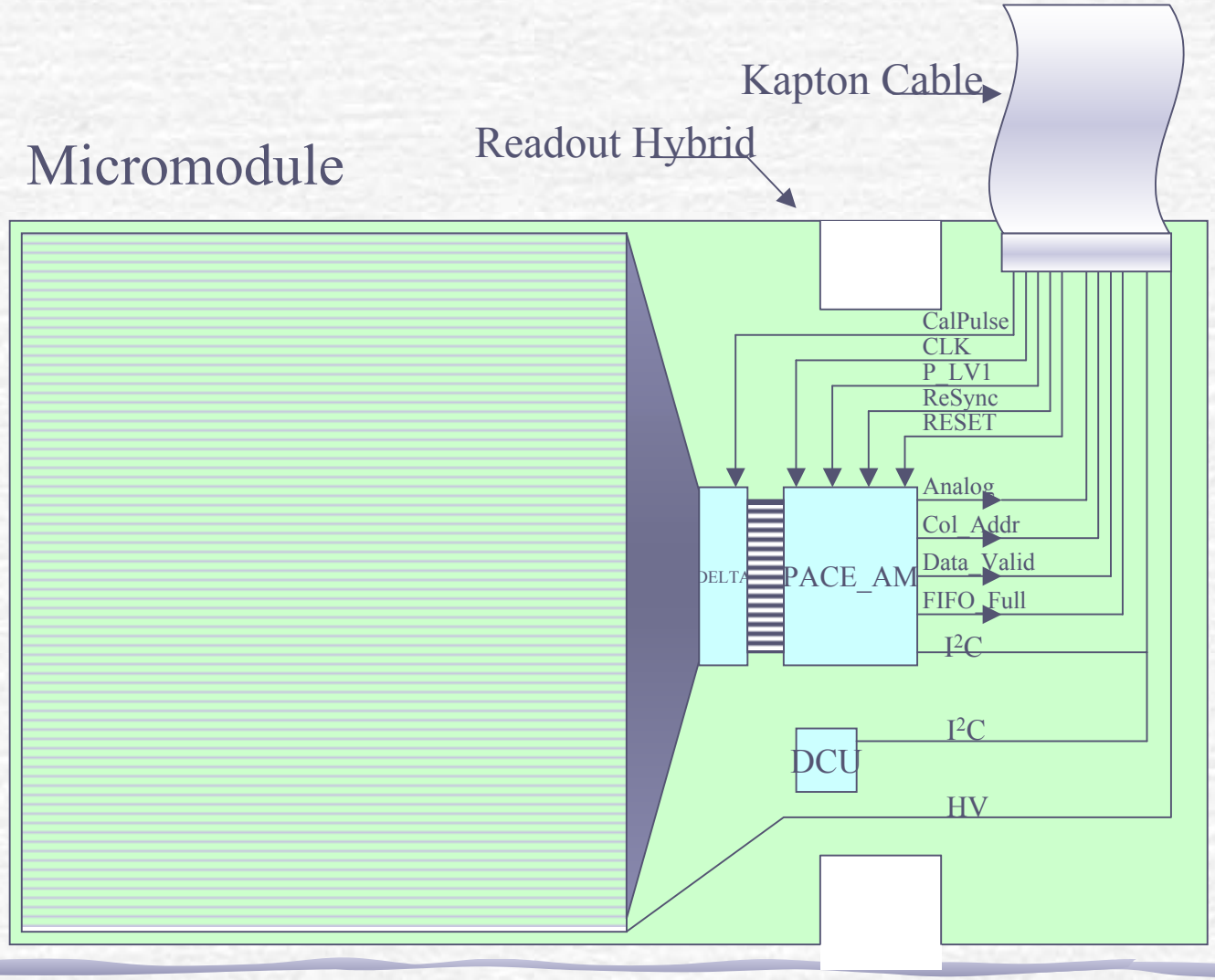
Version: 0.1 DRAFT

Date: February 21, 2001

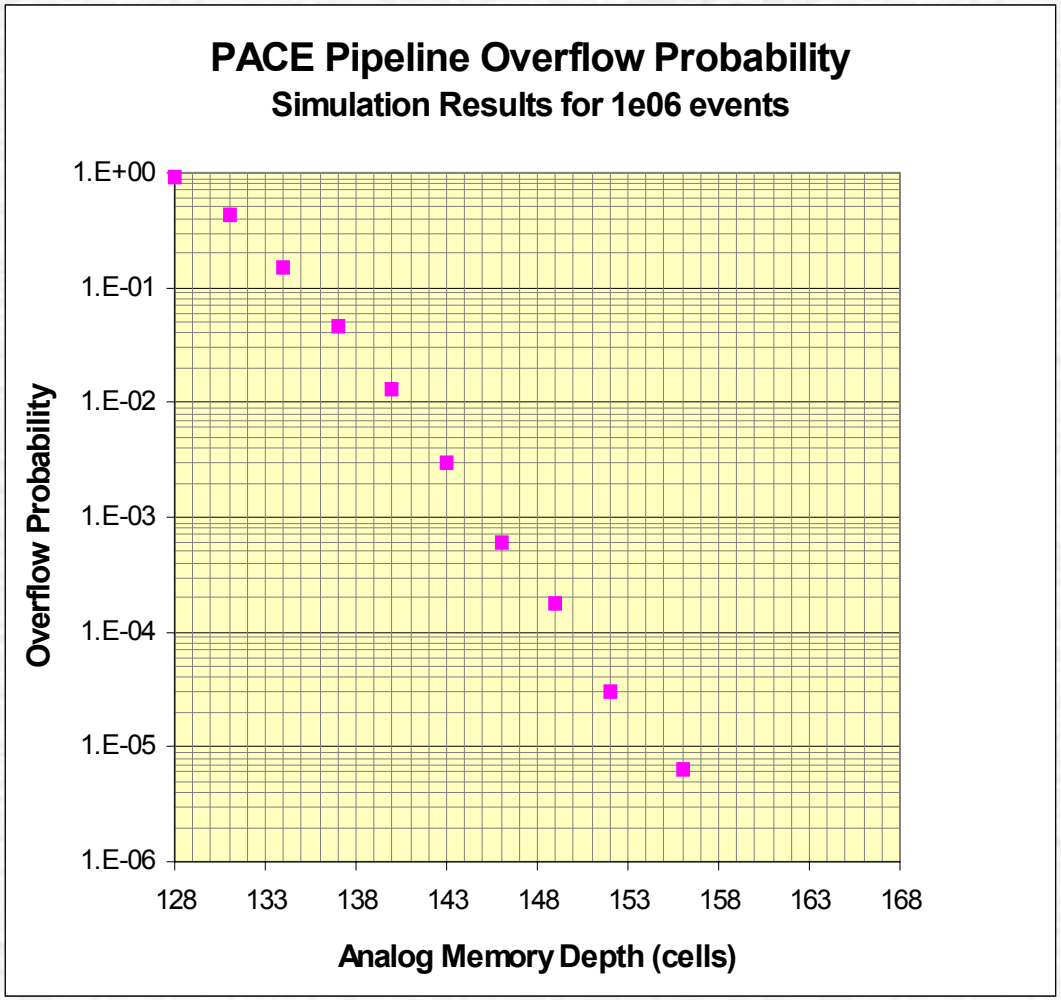
Last Update: May 10, 2001

Notes: This document is a draft for people working on the CMS Preshower Readout and control System and serves as preliminary specifications for the system.
Please check regularly for updates.

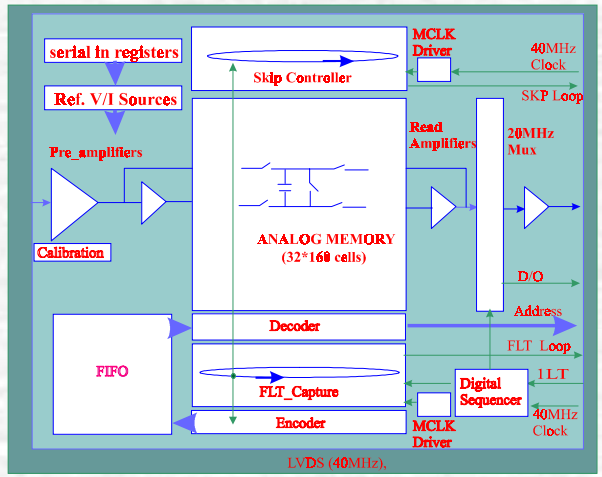
Micromodule



Front-End Pipeline Overflow

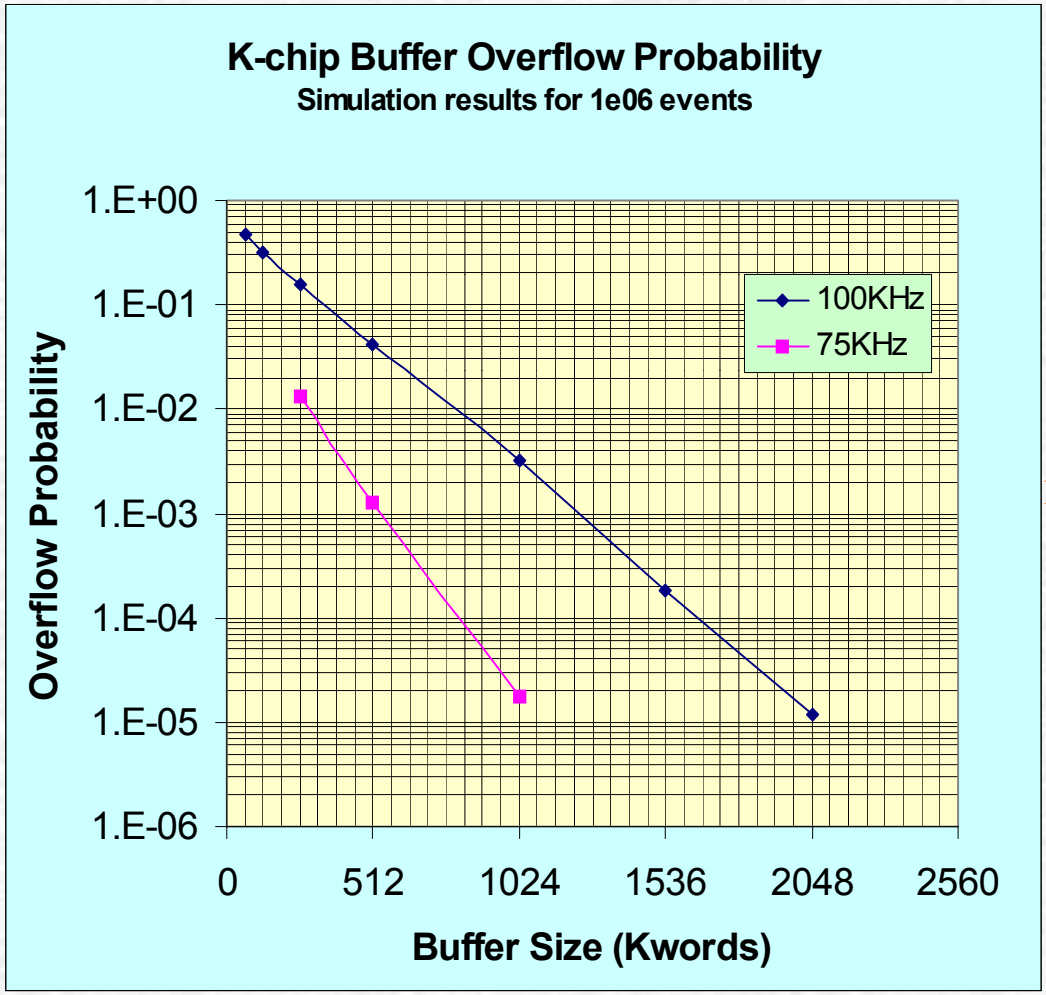


- Pipeline size
- Trigger Latency : 128 cells
- FIFO size : 8*3 cells
- Overhead : 8 cells
  = 160 cells
- *Overflow Probability: ~2e-06*



- Samples per Event: 3
- Channels MUXed in: 32
- Trigger Rate: 100KHz
- MUX Freq. : 20 MHz

K-chip Buffer Size



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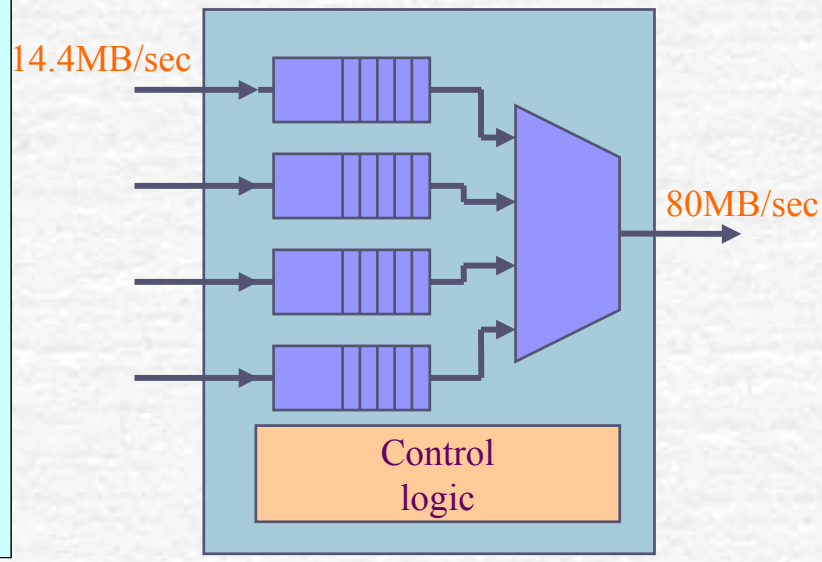
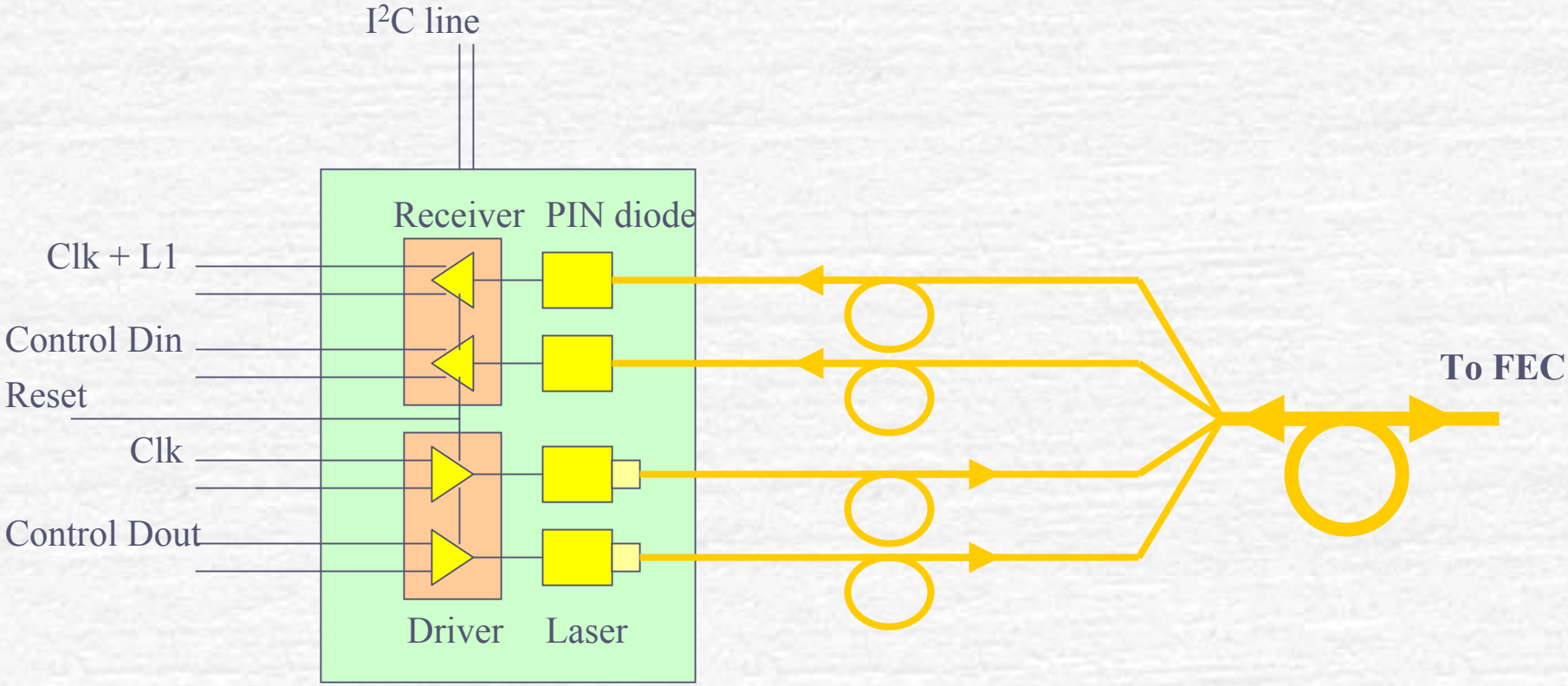


Digital Optical Hybrid



DOH (Digital Optical Hybrid)