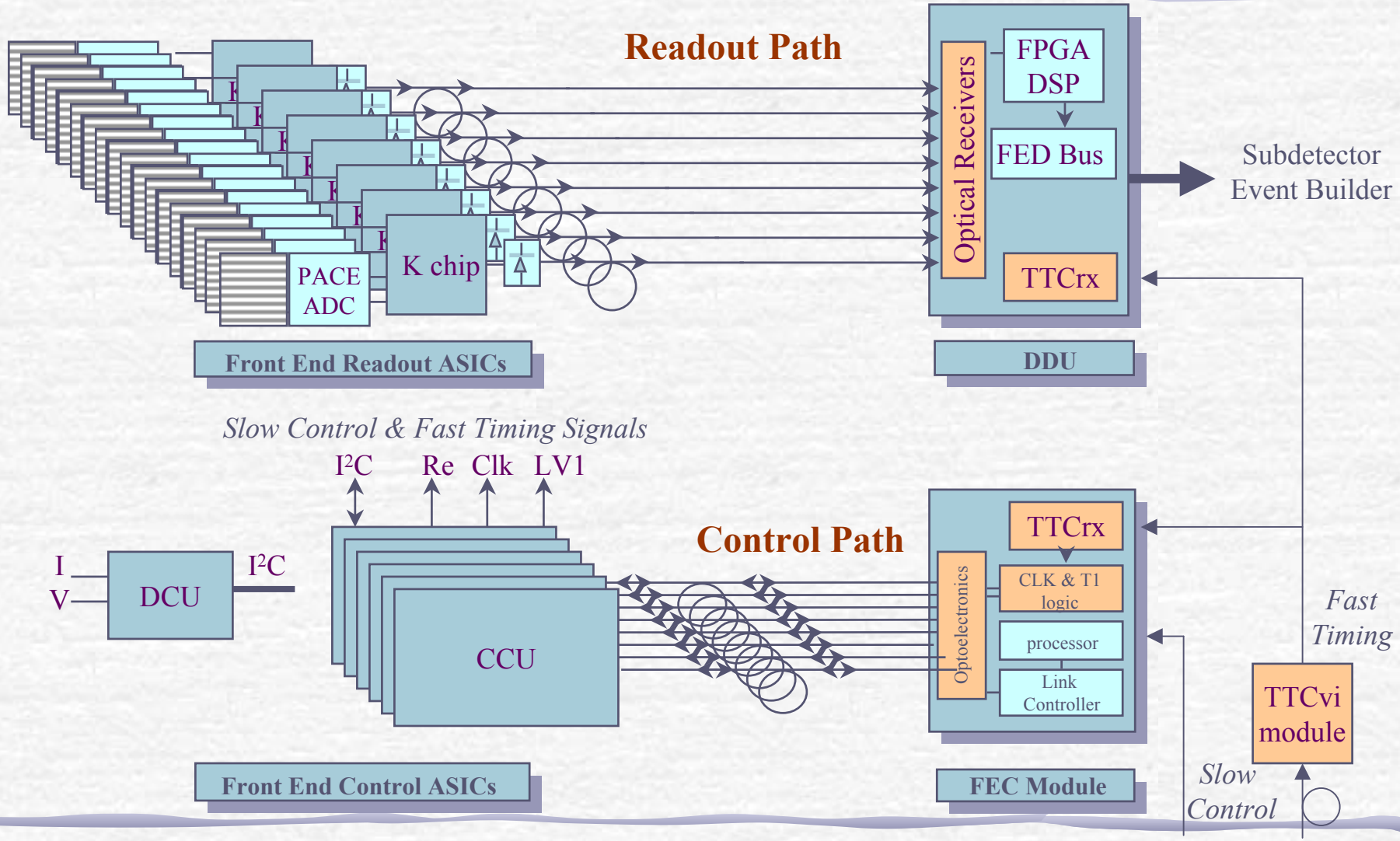
PRESHOWER Front-End System

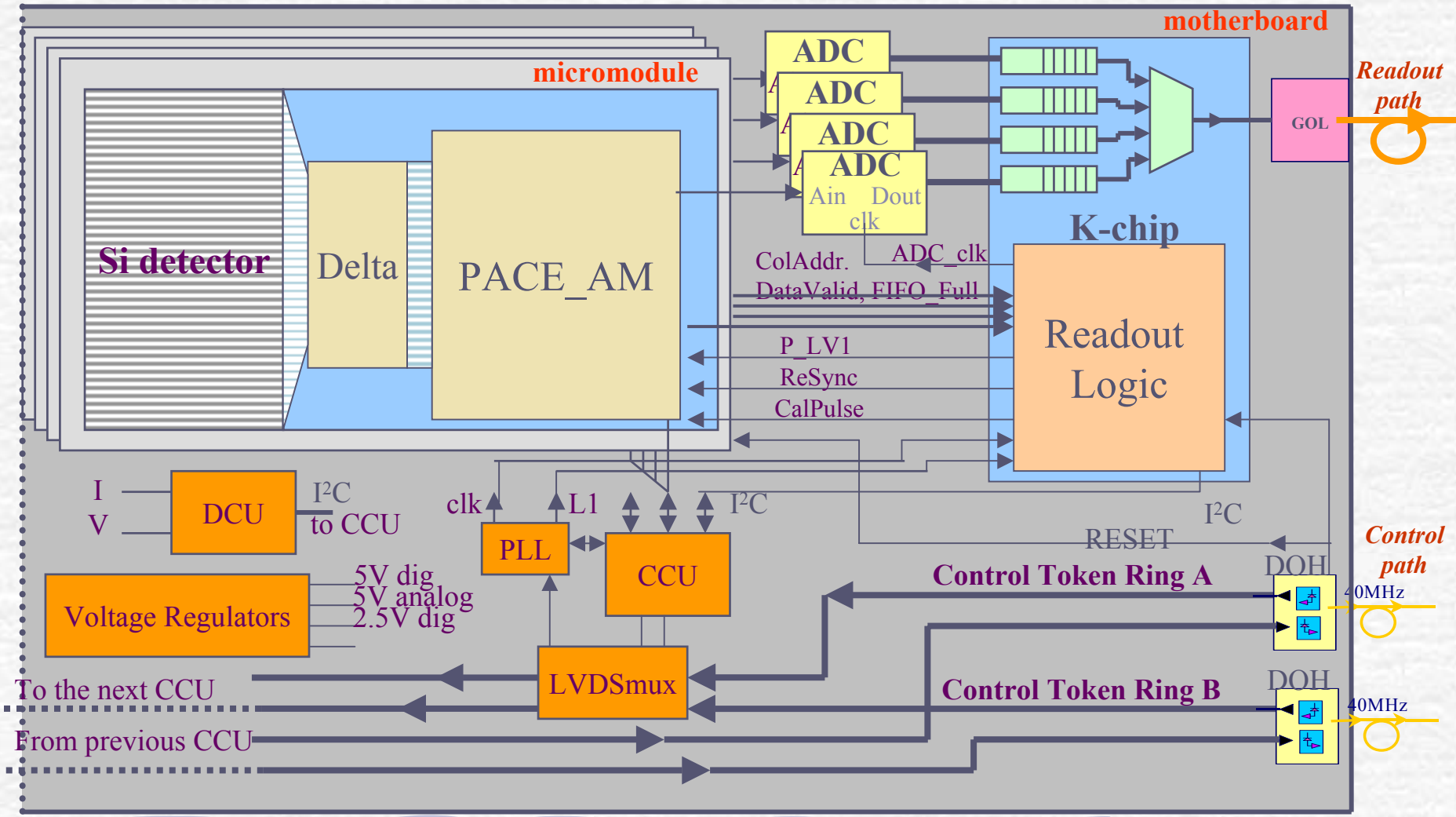
CMS Electronics Week
May 2002

KLOUKINAS Kostas
EP/CME-PS

General Readout & Control Architecture



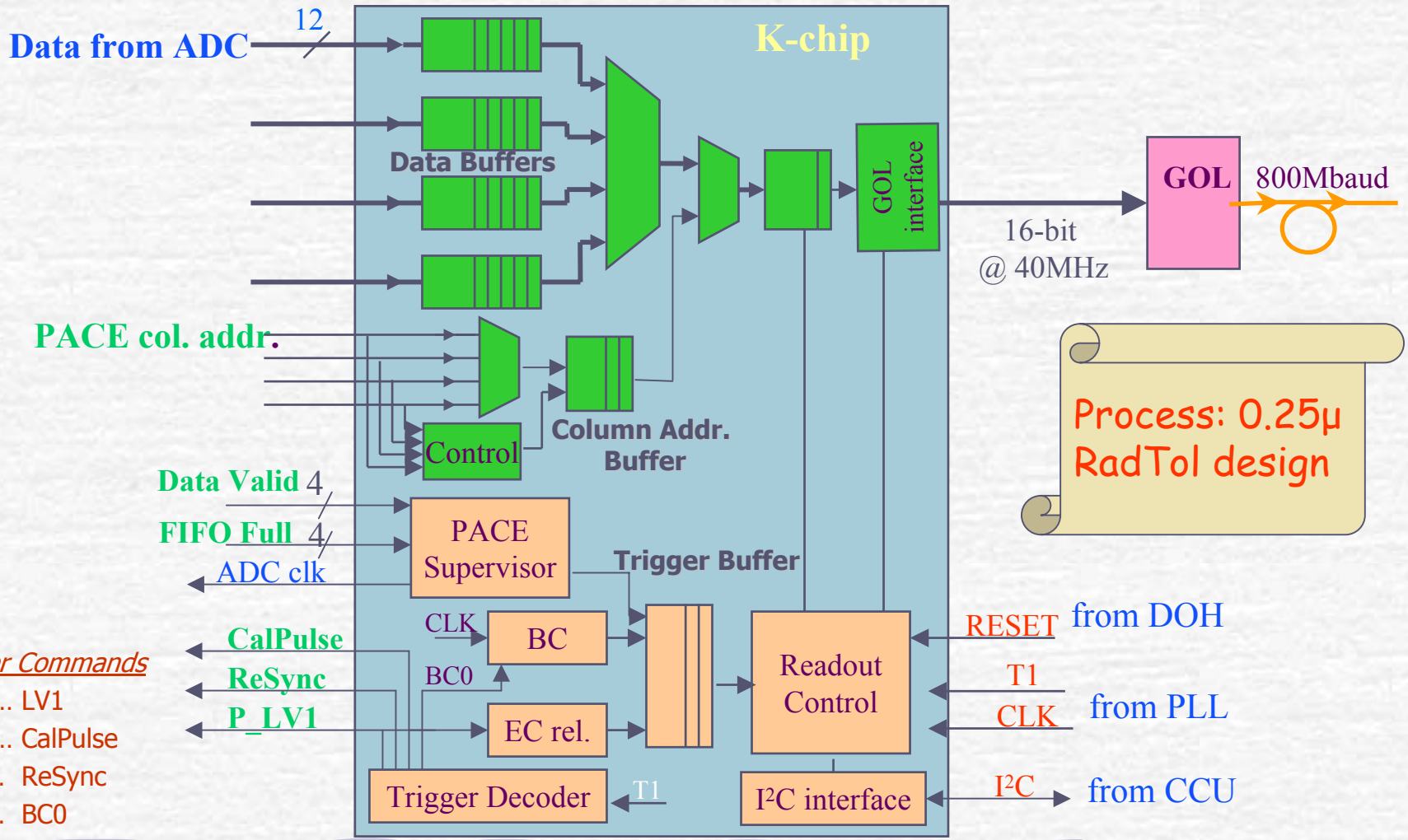
Front End Block Diagram



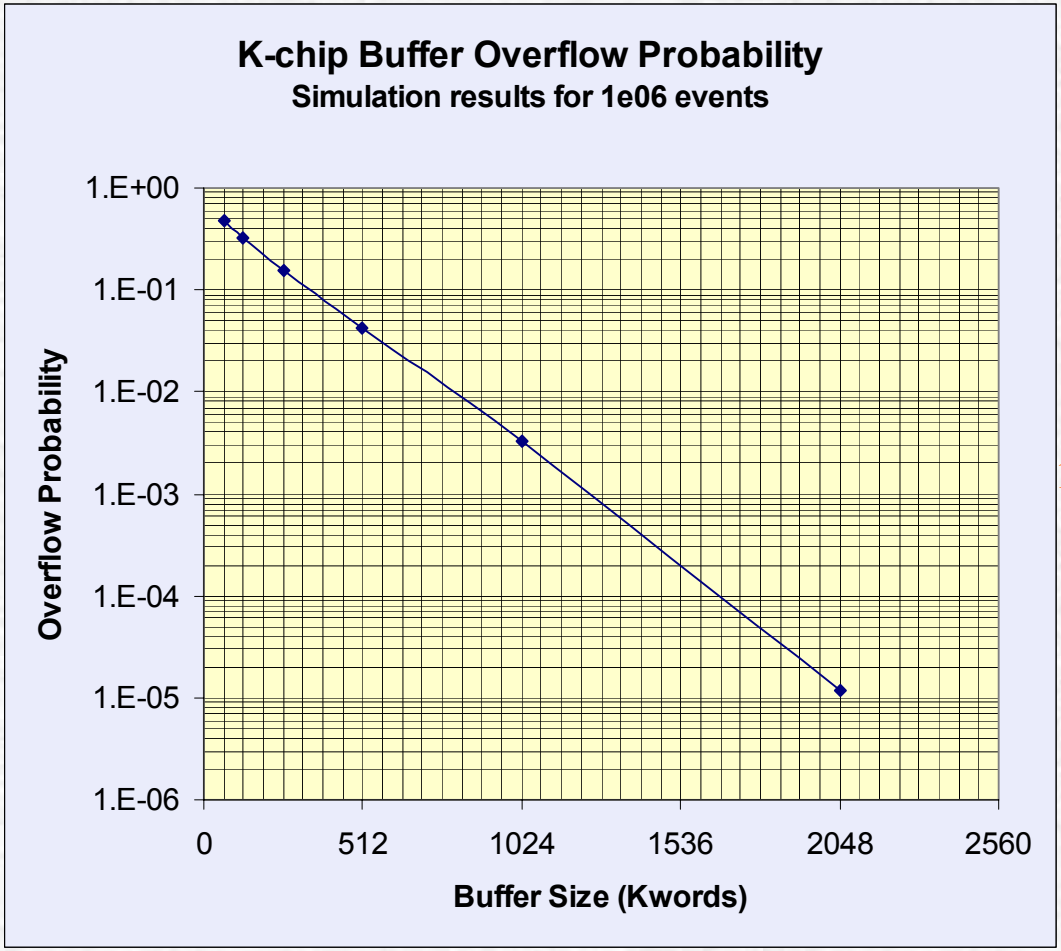
K-chip Functionality

- PACE Readout Control
  - Data concentration from 4 PACE chips
  - Event Buffering
  - No Zero Suppression
  - Bunch Crossing Identification
- Event Data Formatting
  - Data alignment into 16-bit words
  - Data Packet formatting
- Data Transmission over the Gigabit Optical Link
- Buffer Overflow Handling
  - Trigger Inhibit Logic (programmable)
  - Null Event Insertion
- Trigger Decoder Logic
- Front End Clock Distribution
  (40MHz PACE clock, 20MHz ADC clock)

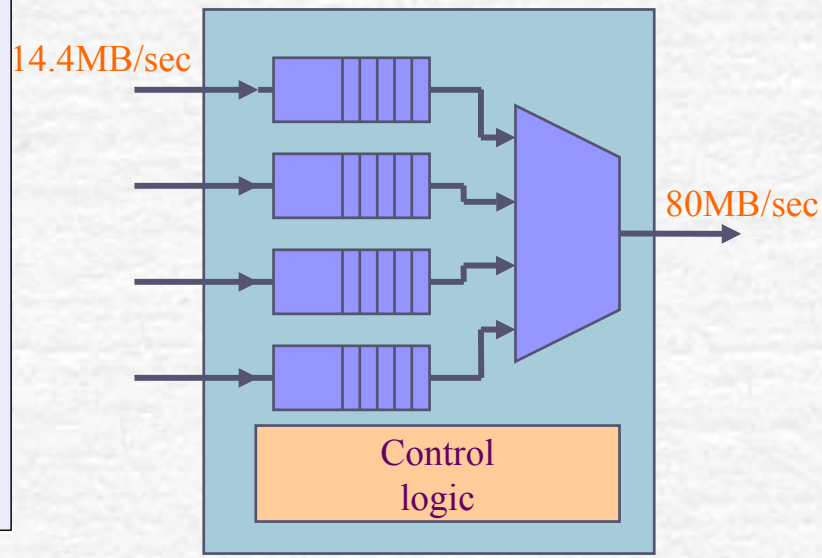
K-chip Block Diagram



K-chip Buffer Size



- Samples per Event: 3
- Channels MUXed in: 32
- Trigger Rate: 100KHz
- Link Throughput: 640Mbps



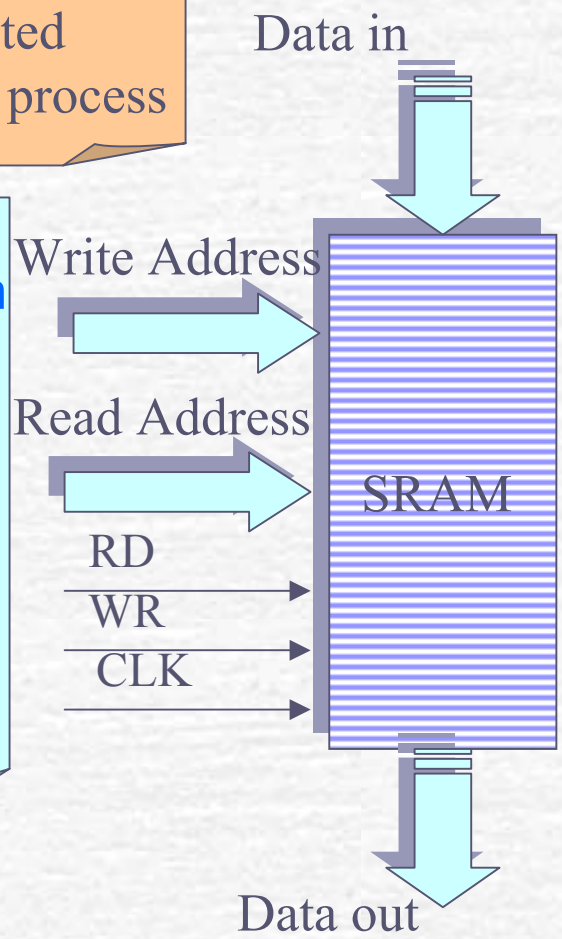
SRAM Features

Motivation: No SRAM design existed for the CERN Radiation Tolerant 0.25μ process

Design Specifications

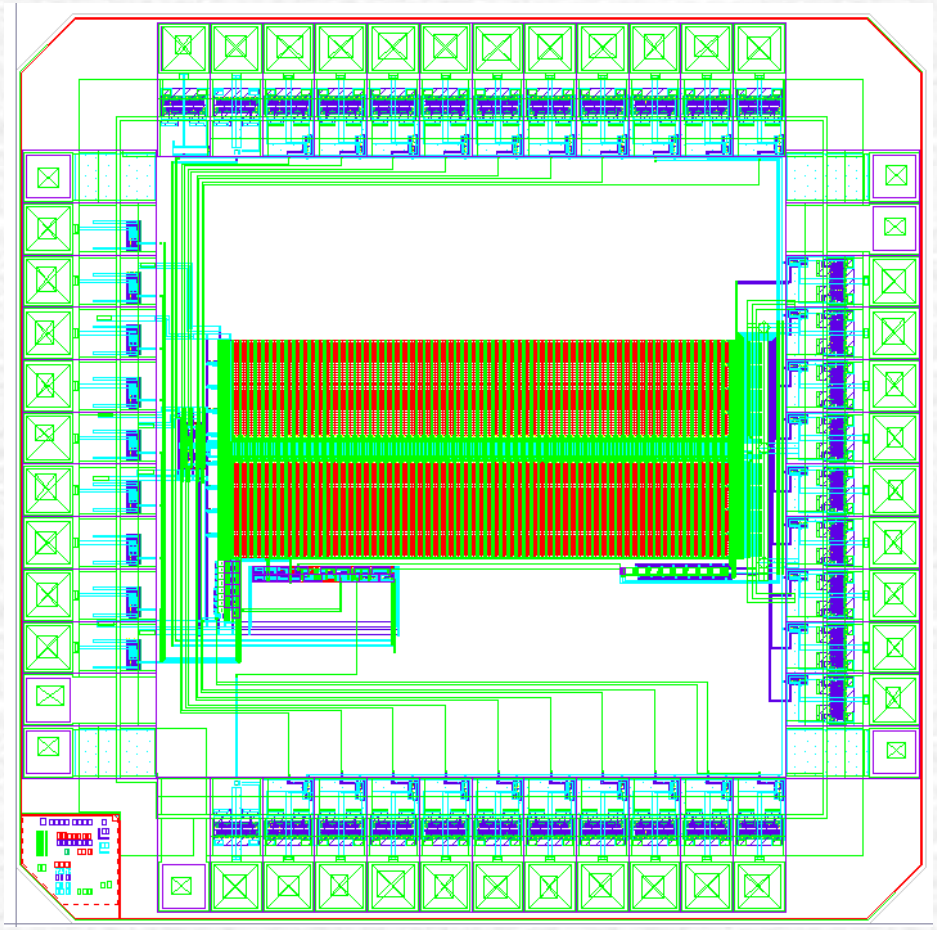
- **Synchronous *pseudo* Dual Port Operation**
- **Operating frequency: 40MHz**
- **Flexible configuration of memory size !**
- **Radiation Tolerant Design**

- **Data bus width: (n x 9)bits**
- **Data arrangement: 8 bit + 1 parity bit**
- **Memory Size: up to 4K words**
- **Registered Inputs, Latched outputs**



Submitted SRAM Chips

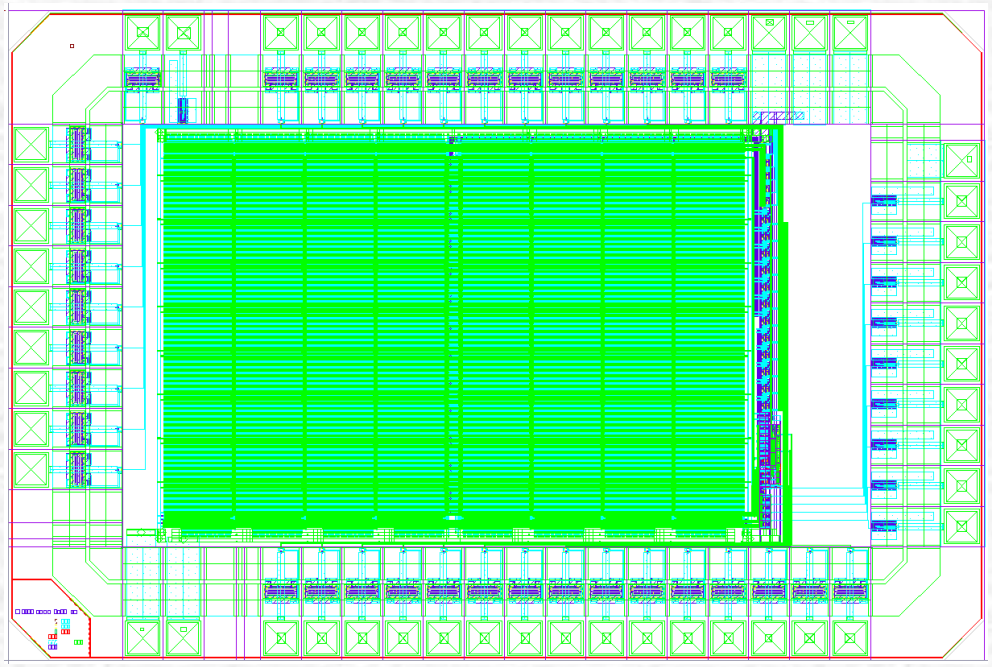
- 1st Prototype (CERN MPW 4)
- Configuration: 1Kx9 bit
- Size: ~560μm x 1,300μm
- Area: ~0.73mm²
- Submitted: Oct. 2000.
- Chip Received: Feb 2001
- Tested: Apr. 2001
- Status: O.K.



Design: CERN_SRAM_1K
Designer: Kloukinas Kostas
EP/CME-PS

Submitted SRAM Chips

- 2nd Prototype (CERN MPW 5)
- Configuration: 4Kx9 bit
- Size: ~1,850μm x 1,300μm
- Area: ~2.4mm²
- Submitted: May 2001
- Chip Received: Aug. 2001
- Tested: Oct. 2001
- Status: O.K.



Design: CERN_SRAM_4K
Designer: Kloukinas Kostas
EP/CME-PS

CERN SRAM test results

- Functional tests (4Kx9bit SRAM)
  - Max operating frequency: 60MHz @ 2.5V
  - Read access time: 7.6ns @ 2.5V
  - Power dissipation: 15μW / MHz @ 2.5V for simultaneous R/W access cycles (0.60mW @ 40MHz).
  - Design tested for process variations: -3σ, –1.5σ, typ, +1.5σ, +3σ
- Irradiation tests
  - Total ionizing dose: up to 10MRad
    - No increase in power dissipation.
    - No degradation in performance.
  - Single Event Upsets: under preparation (in collaboration with EP/MIC group)

K-chip Design Status & Planning

- Data Path is implemented using SRAM modules.
- Control Logic is implemented in synthesizable Verilog code.

- 1st Design Review in March 2002
  - Some changes were requested.
    - PACE - Kchip interface synchronization
    - Buffer overflow handling
    - Protection of control logic against SEUs

- 2nd Design Review in June 2002

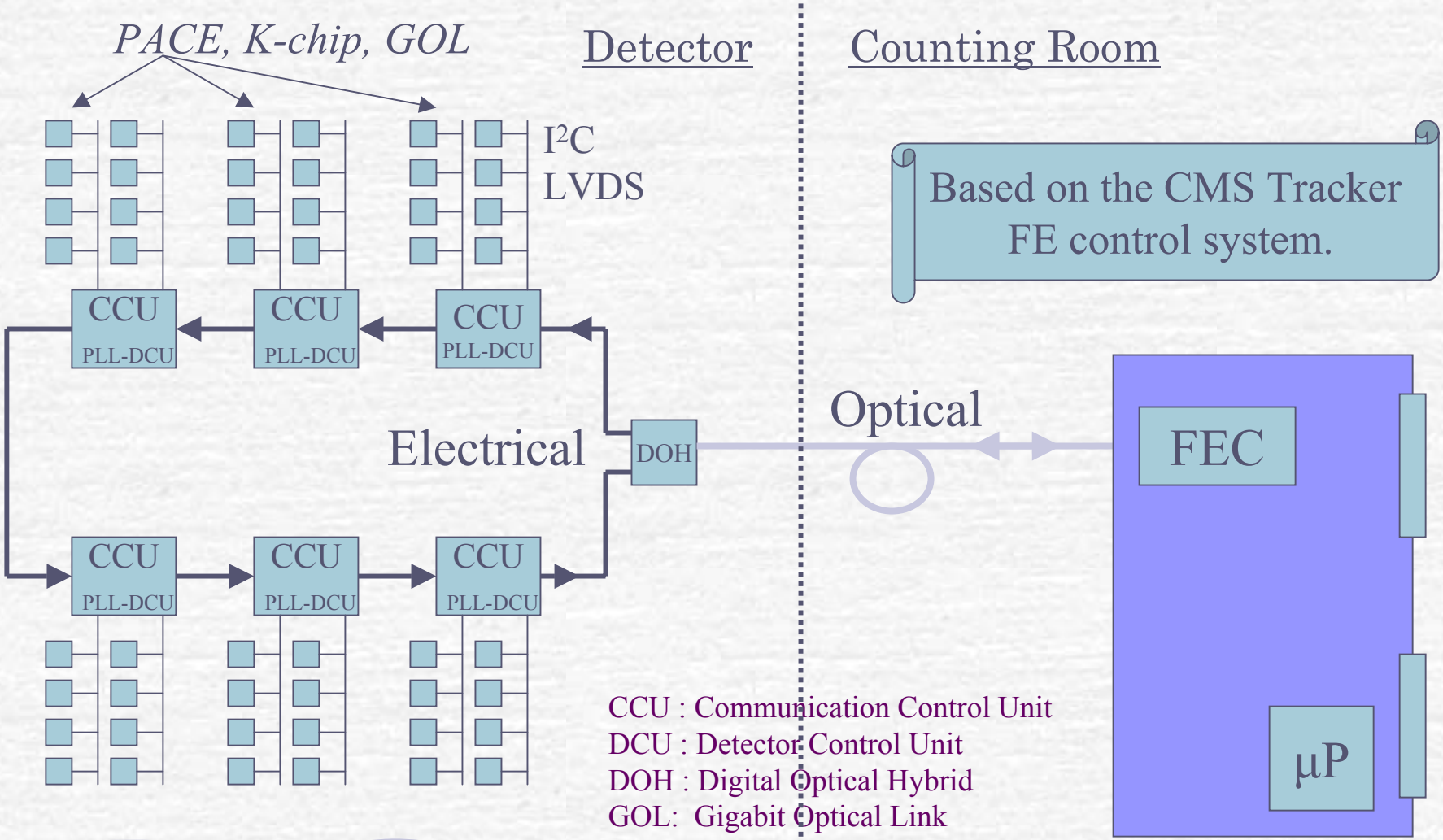
- Target submission: CERN MPW 8 (Aug. 2002)

- Pending system issues affecting K-chip design:
  - the operation mode of the GOL and
  - the clock stability for driving the GOL chip

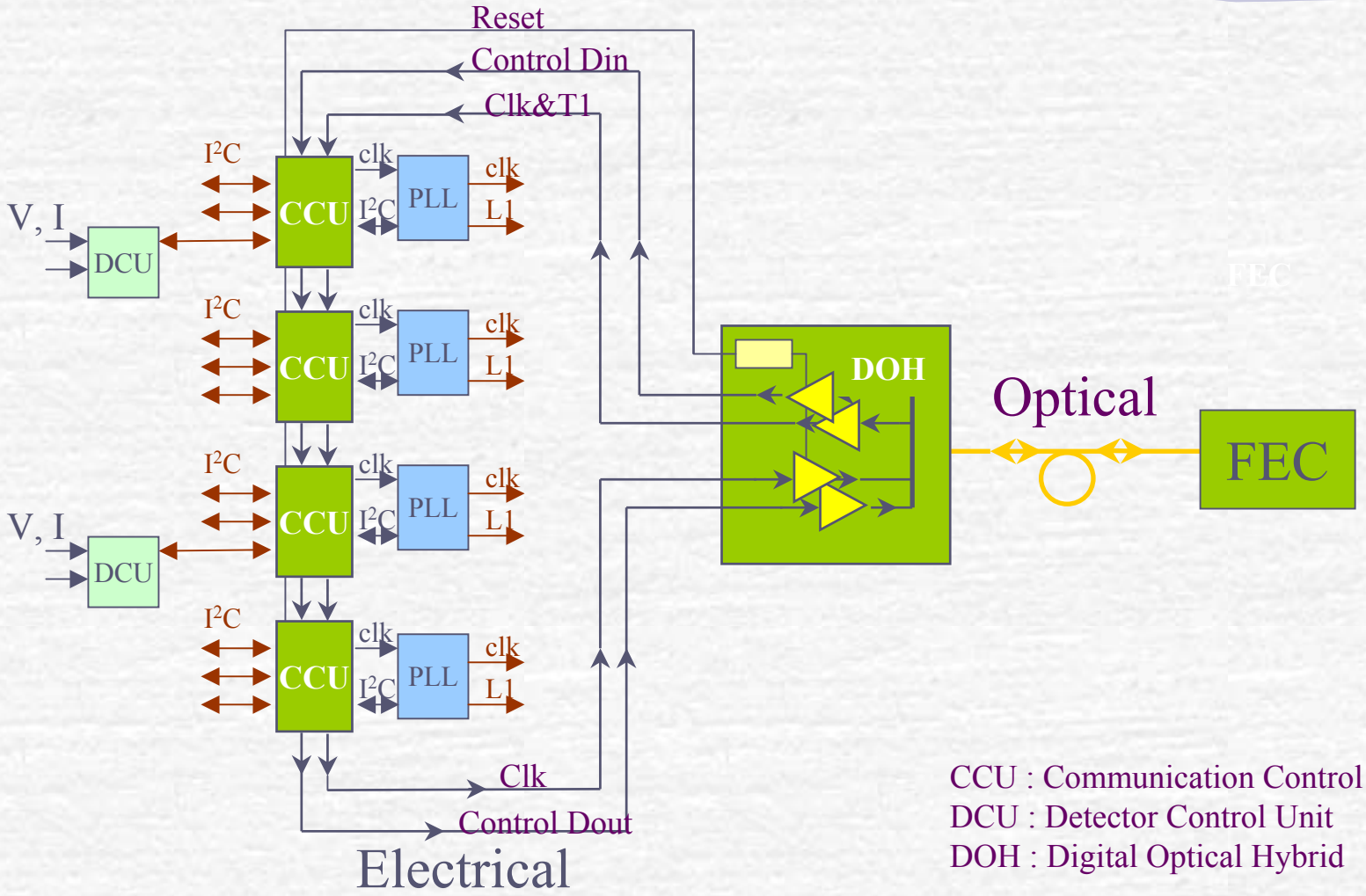
Front-End Control System

- The tasks of the Preshower Front-End Control System are to distribute to the detector embedded electronics:
  - Fast Synchronizing signals and timing information (LHC clock, LV1 trigger, ReSync, BC0) and
  - Slow control information for controlling the status of the detector, monitoring environmental parameters, front-end electronics set-up and calibration and downloading operating condition parameters.
- A derivative of the **CMS Tracker control system** reusing the ASICs and optoelectronic components developed for the Tracker control system.

Control System Overview

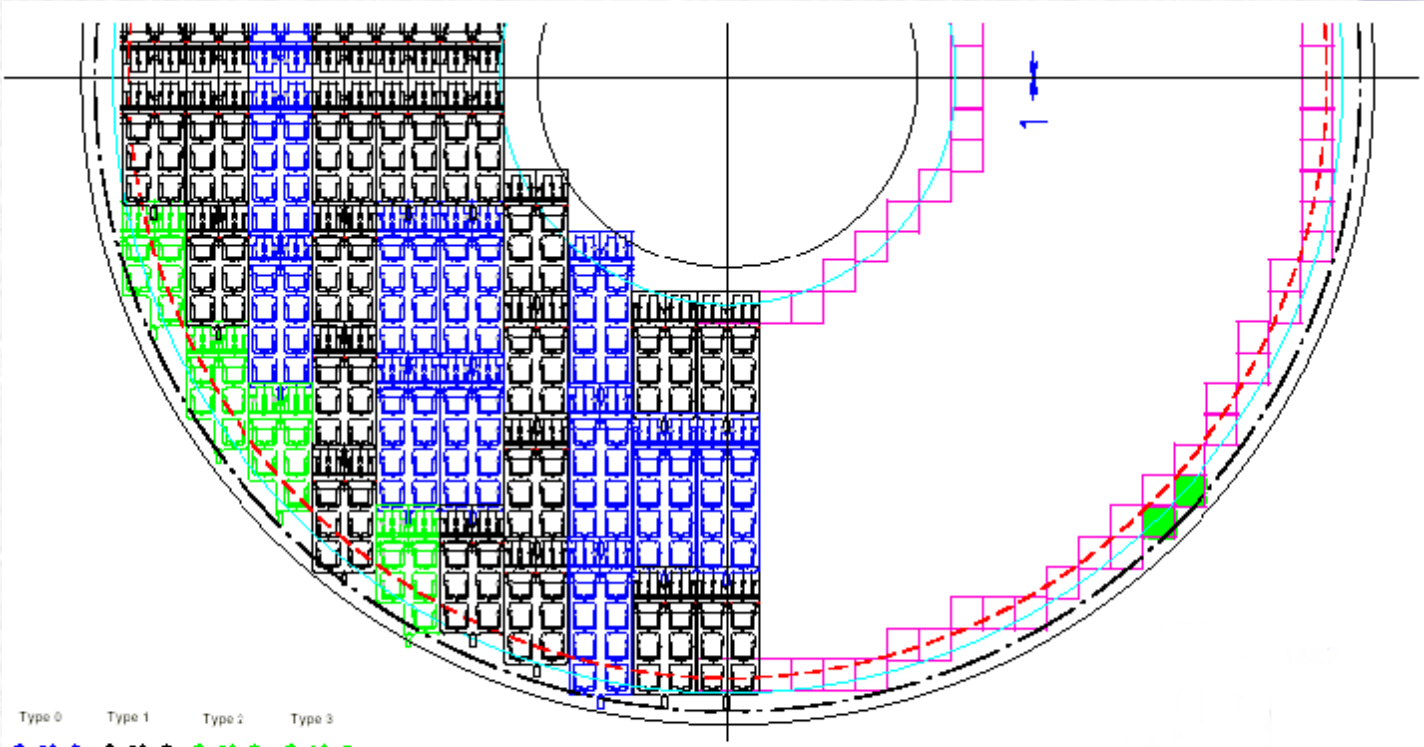


Preshower Control System



CCU : Communication Control Unit
DCU : Detector Control Unit
DOH : Digital Optical Hybrid

Preshower Endcap

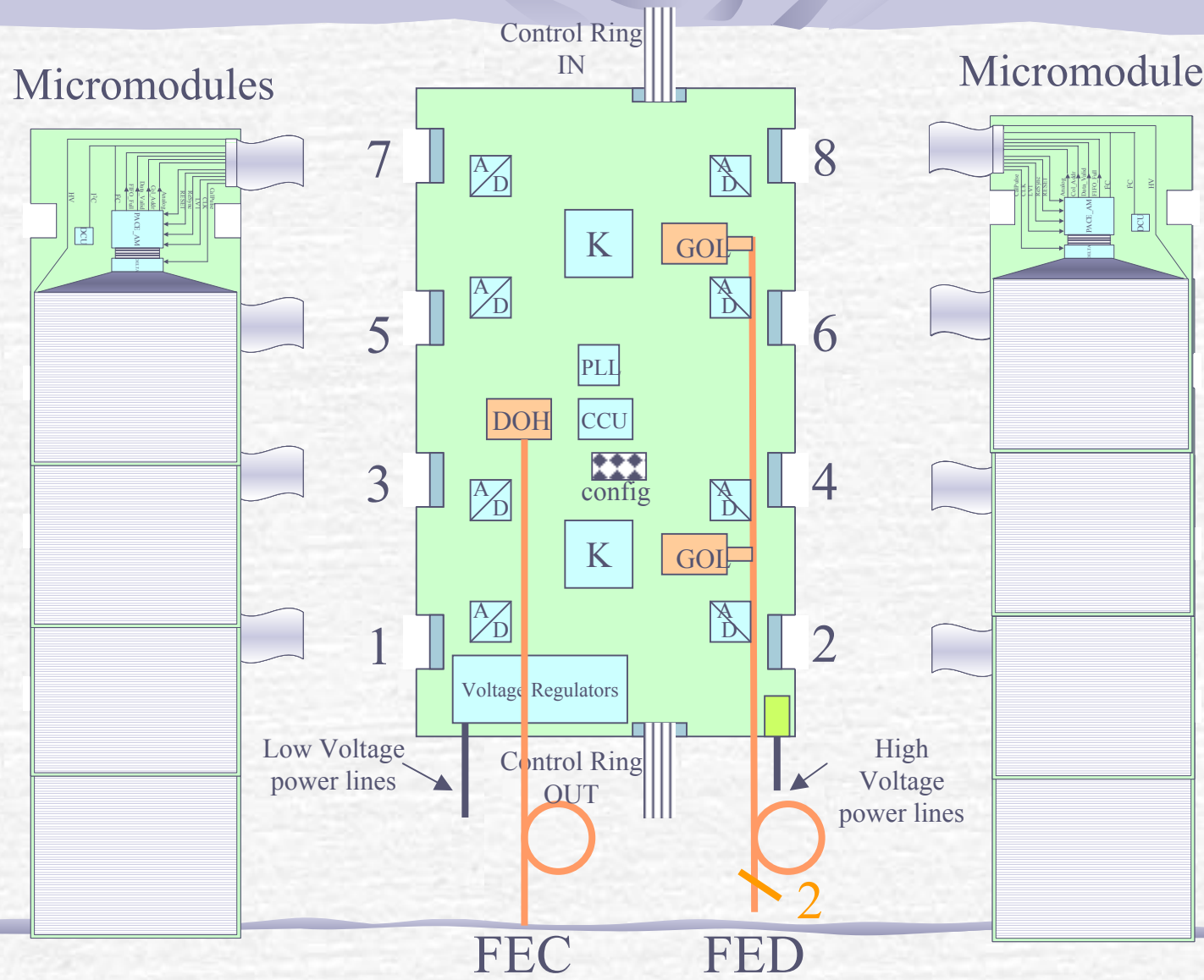


Per read-out plane	2 Endcaps
type 0: 42x	4x42=168
type 1: 68x	4x68=272
type 2: 8x	4x8 =32
type 3: 8x	4x8 =32
126	504 Pcs.

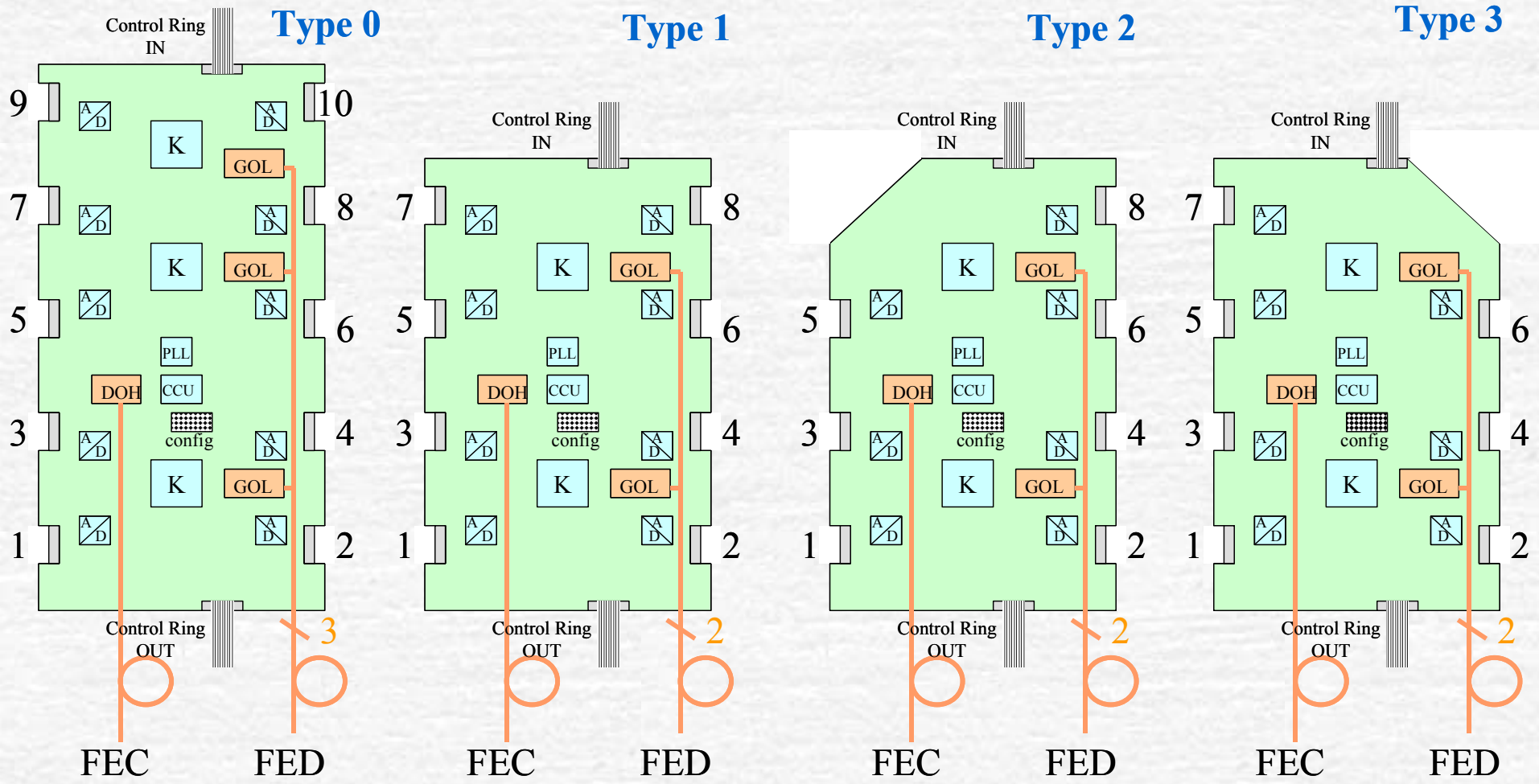
	Links per ladder	Number of Links
type 0	3	3x168 = 504
type 1	2	2x272 = 544
type 2	2	2x 32 = 64
type 3	2	2x 32 = 64

Total number of links = 1176

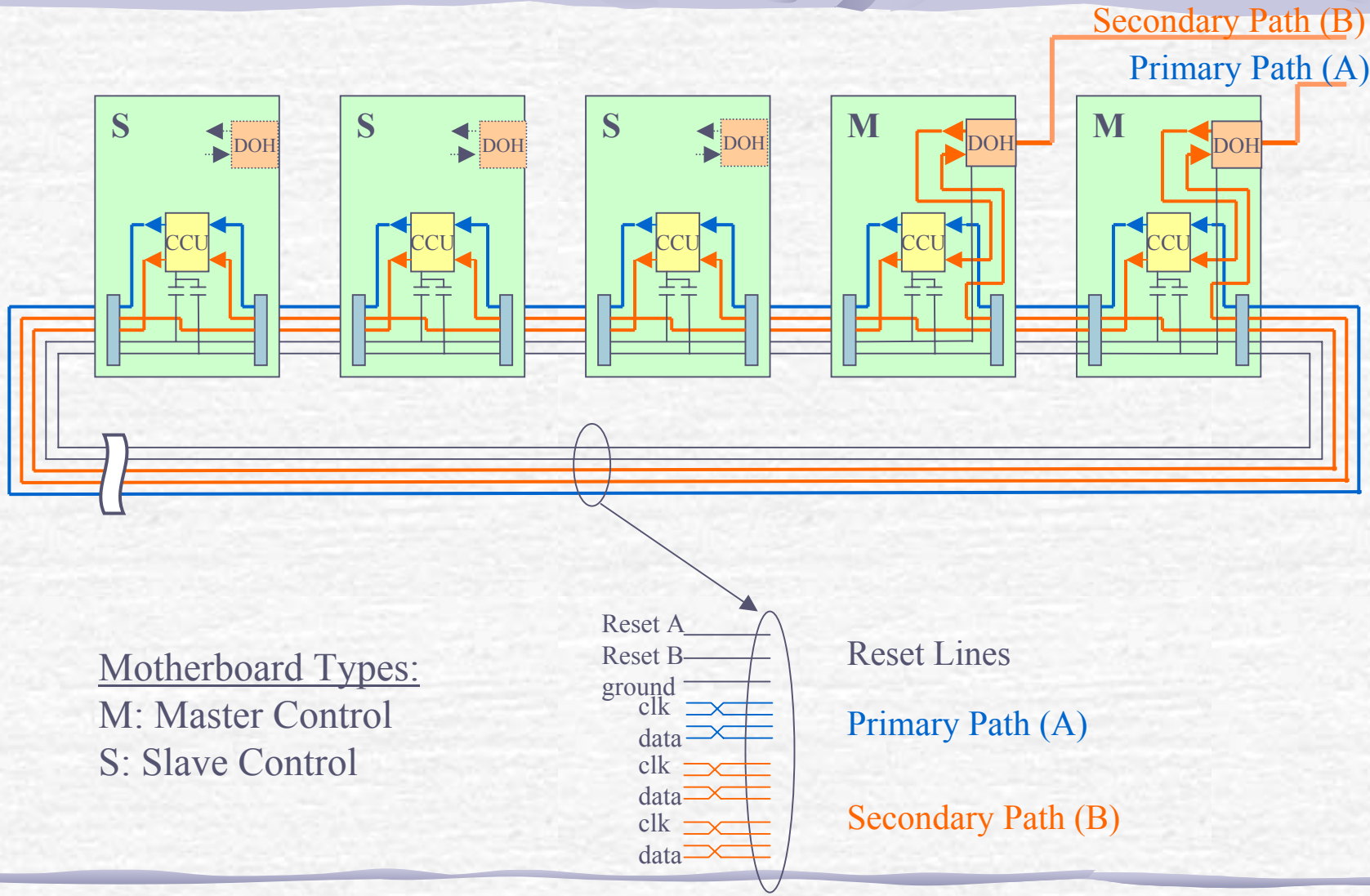
Motherboard



Motherboard Types



Motherboard Interconnection



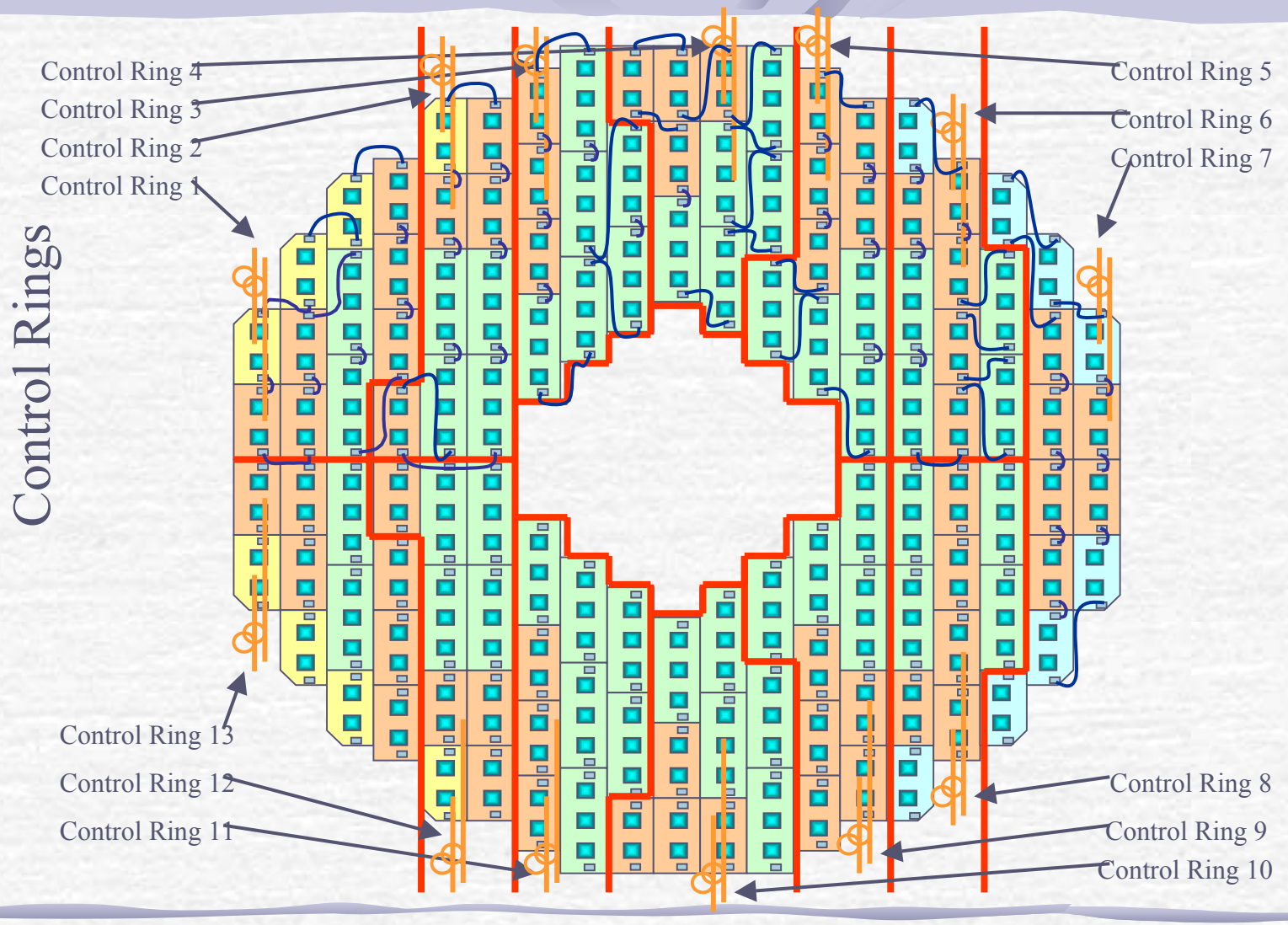
Motherboard Types:
M: Master Control
S: Slave Control

Reset Lines

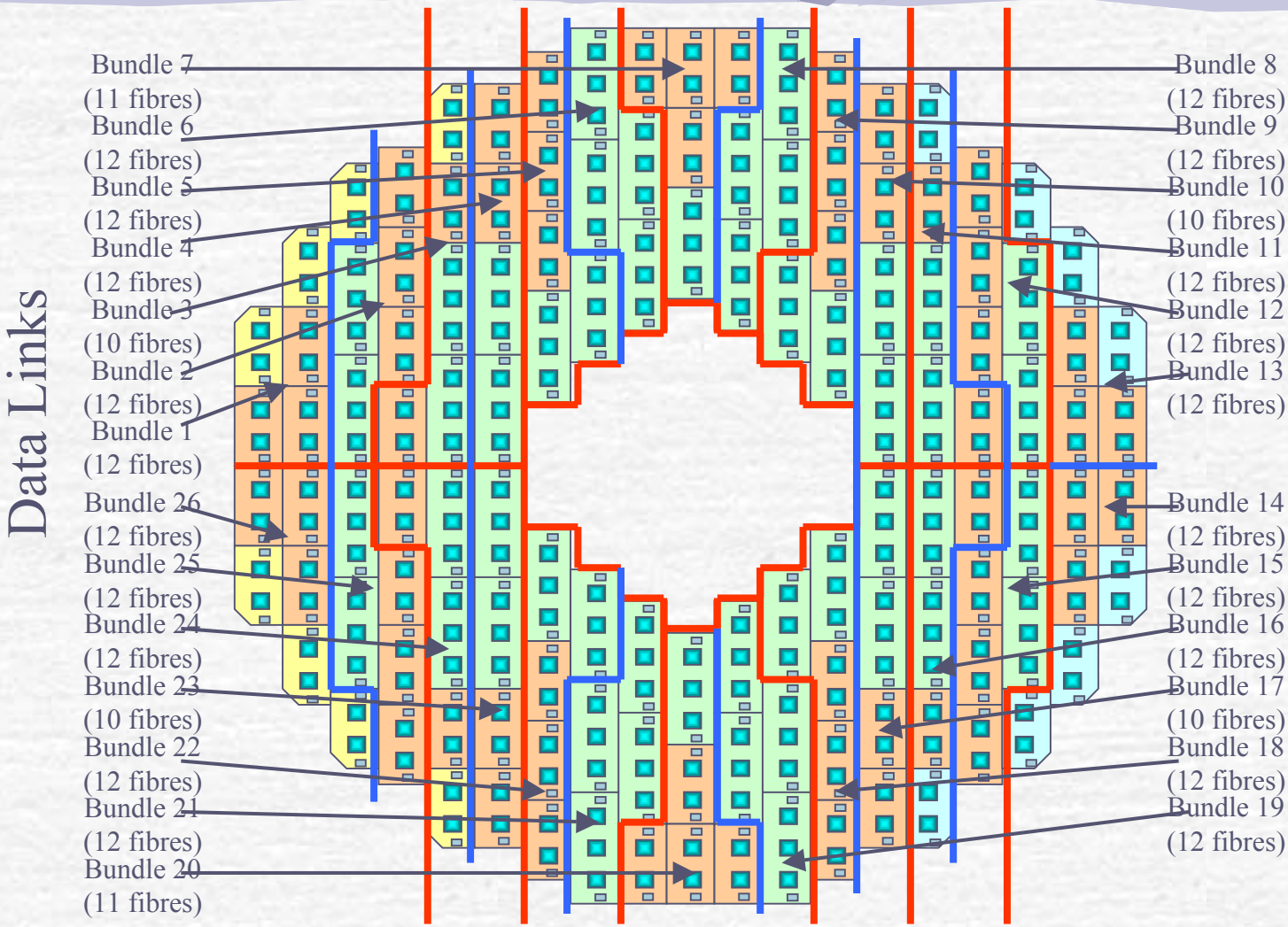
Primary Path (A)

Secondary Path (B)

Control Links



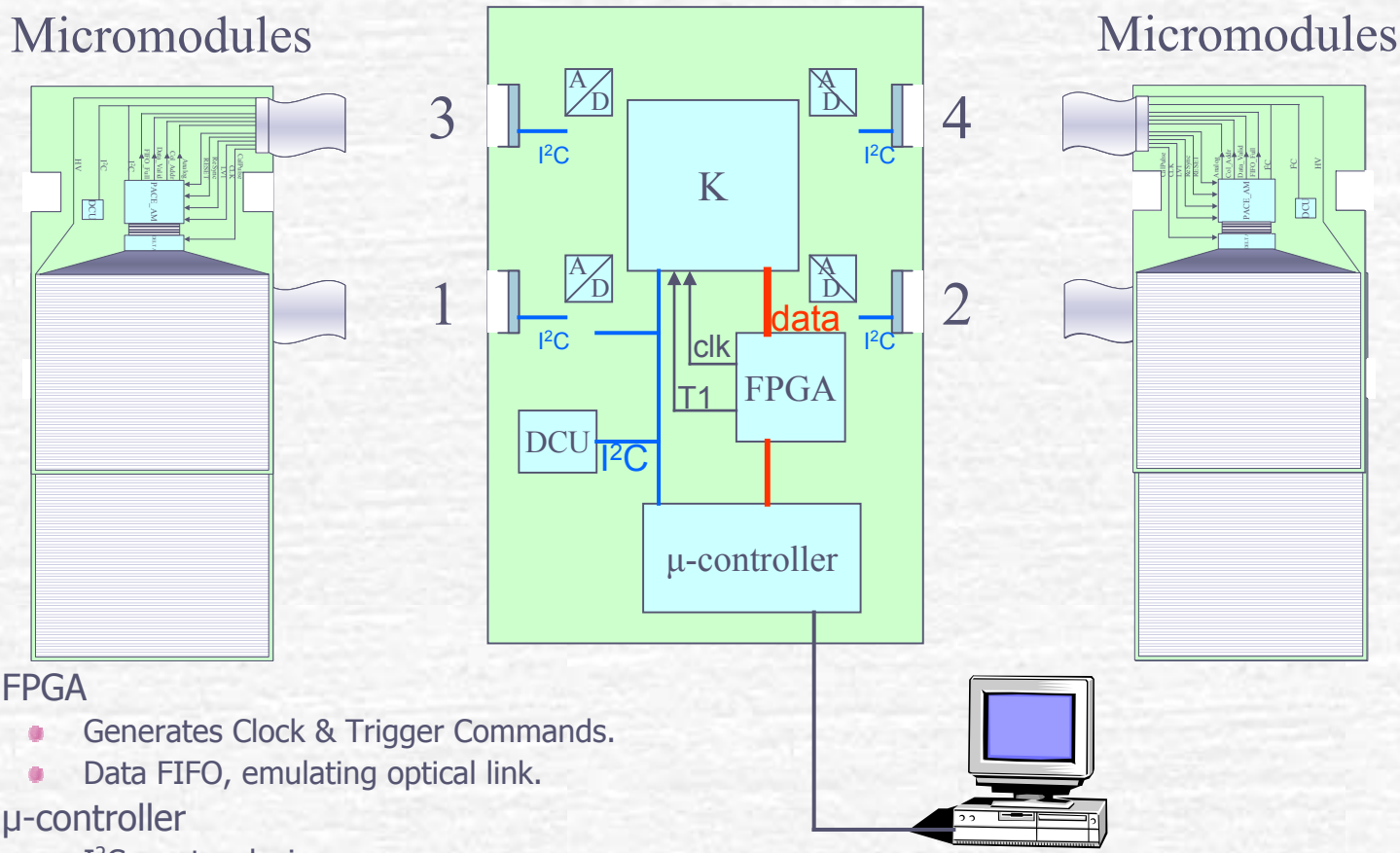
Data Links


Data Links
Bundle 7
(11 fibres)
Bundle 6
(12 fibres)
Bundle 5
(12 fibres)
Bundle 4
(12 fibres)
Bundle 3
(10 fibres)
Bundle 2
(12 fibres)
Bundle 1
(12 fibres)
Bundle 26
(12 fibres)
Bundle 25
(12 fibres)
Bundle 24
(12 fibres)
Bundle 23
(10 fibres)
Bundle 22
(12 fibres)
Bundle 21
(12 fibres)
Bundle 20
(11 fibres)
Bundle 8
(12 fibres)
Bundle 9
(12 fibres)
Bundle 10
(10 fibres)
Bundle 11
(12 fibres)
Bundle 12
(12 fibres)
Bundle 13
(12 fibres)
Bundle 14
(12 fibres)
Bundle 15
(12 fibres)
Bundle 16
(12 fibres)
Bundle 17
(10 fibres)
Bundle 18
(12 fibres)
Bundle 19
(12 fibres)

FE System Integration

- K-chip Test Motherboard design
  - A reduced version of the System Motherboard.
  - This version will not incorporate the slow control system and the high speed link chip (GOL).
  - It will serve as a test bench for:
    - Evaluating the functionality of the K-chip.
    - Verifying the FE readout system operation.
    - Testing the compatibility of the I2C interfaces of the FE chips (PACE, K-chip, DCU).
    - Testing the interfacing between ASICs powered from different supply voltages.
    - Evaluating the operation of the DCU chip in the Preshower system.
- System Motherboard design
  - First version of the *final system* motherboard.
  - It will include all the slow control ASICs.

K-chip Test Motherboard



- FPGA
  - Generates Clock & Trigger Commands.
  - Data FIFO, emulating optical link.
- µ-controller
  - I²C master device.
  - Data readout controller.

Status & Planning

- K-chip Test Motherboard design
  - Motherboard Design is in advanced stage.
  - Design of a new version of micromodules is progressing.
  - Test system (including FPGA and μ-controller code) is expected to be ready in Nov. 2002.
- System Motherboard design
  - Schematic design has started.
  - Board is expected to be ready by the end of 2002.
- System Motherboard Tests
  - Acquire FEC, TTCvi modules and control link optoelectronics (depending on availability).
  - Develop a minimal version of the DDU.
  - Develop slow control software.
  - Target period: 1st Half of 2003 (depending on available manpower!).