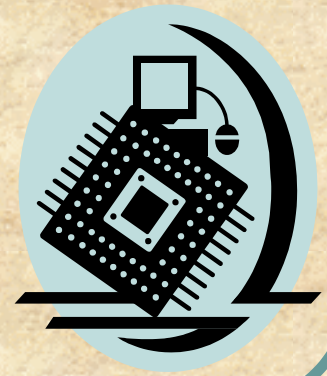
Digital Front-End Electronics

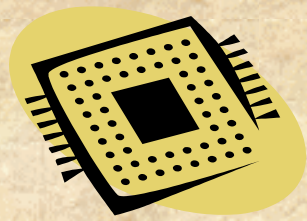
Preshower meeting.

CMS week 3-7 Dec. 2001

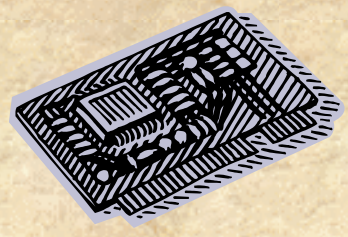


KLOUKINAS Kostas EP/CME-PS

Digital FE electronics activities at CERN

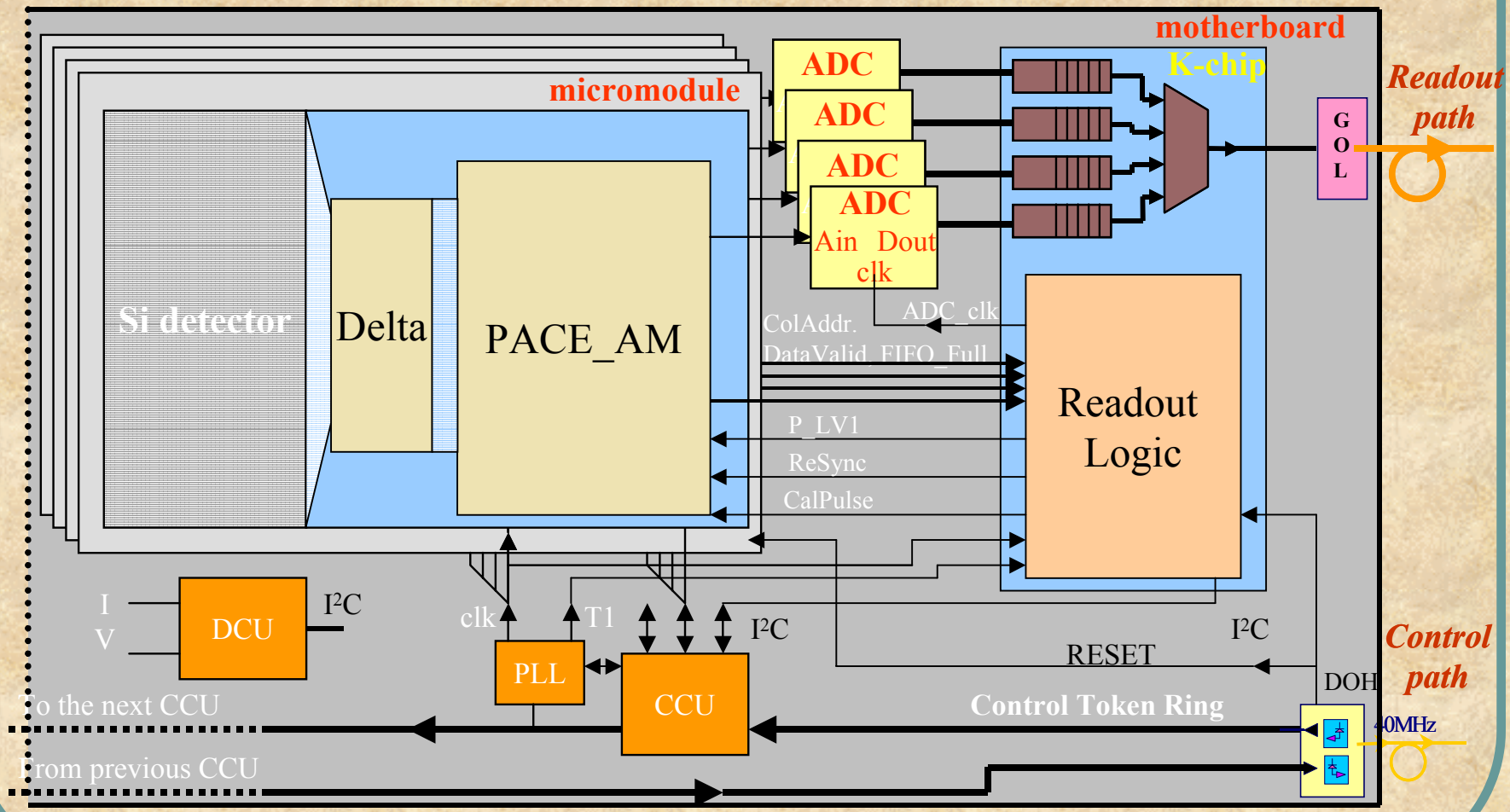


- ASIC design activities
  - K-chip design
    - SRAM design and testing
    - Timing & Control logic design

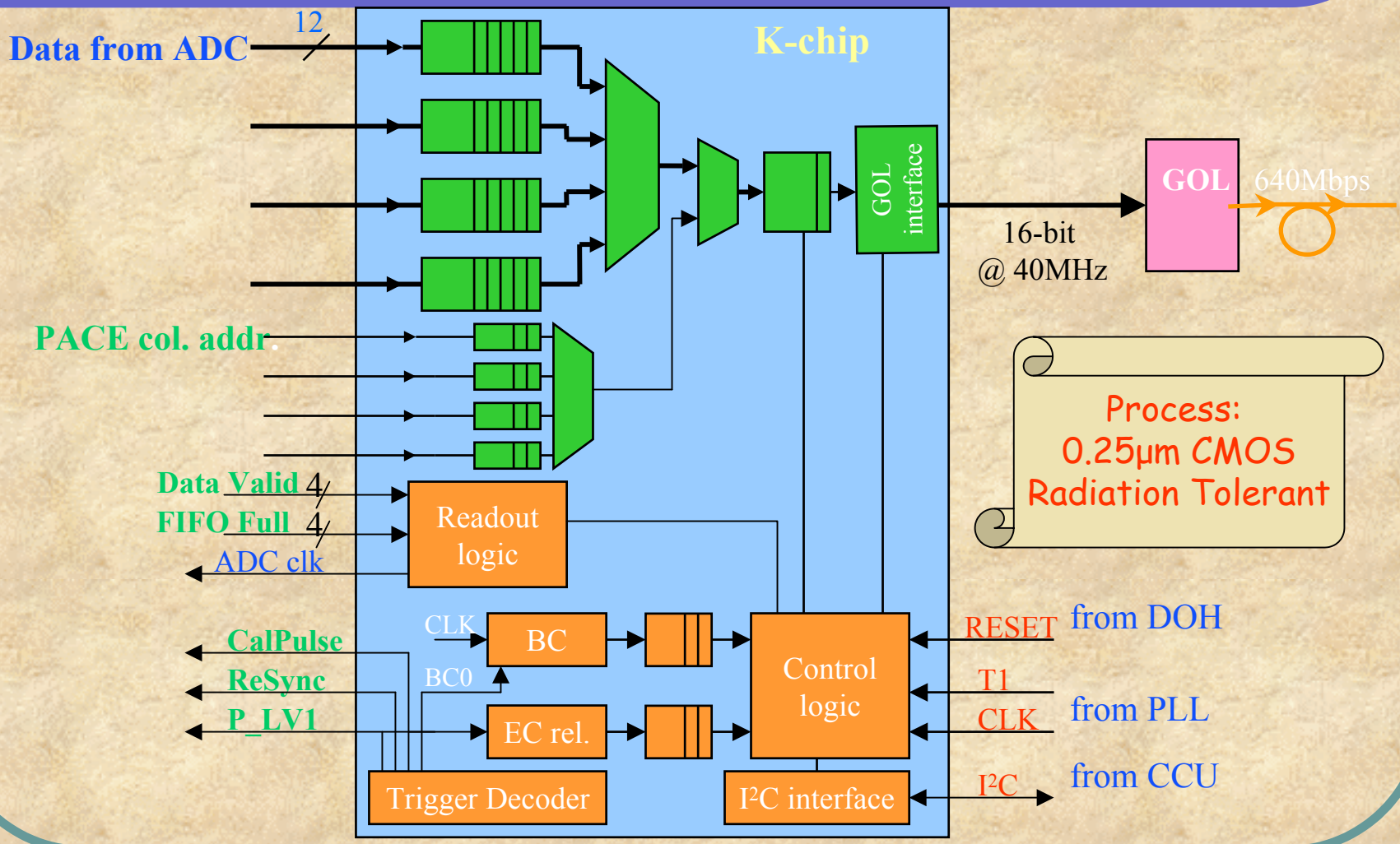


- System level design activities
  - Readout & Control system design
  - Motherboard design
    - K-chip motherboard design.
      A reduced version of the system motherboard.
      It will serve as a test bench for evaluating the K-chip functionality. This version will not incorporate the slow control system and the high speed link chip (GOL).
    - System motherboard design.
      First version of the *final system* motherboard design.
      It will include the high speed link and the slow control system.

Front-end System Overview

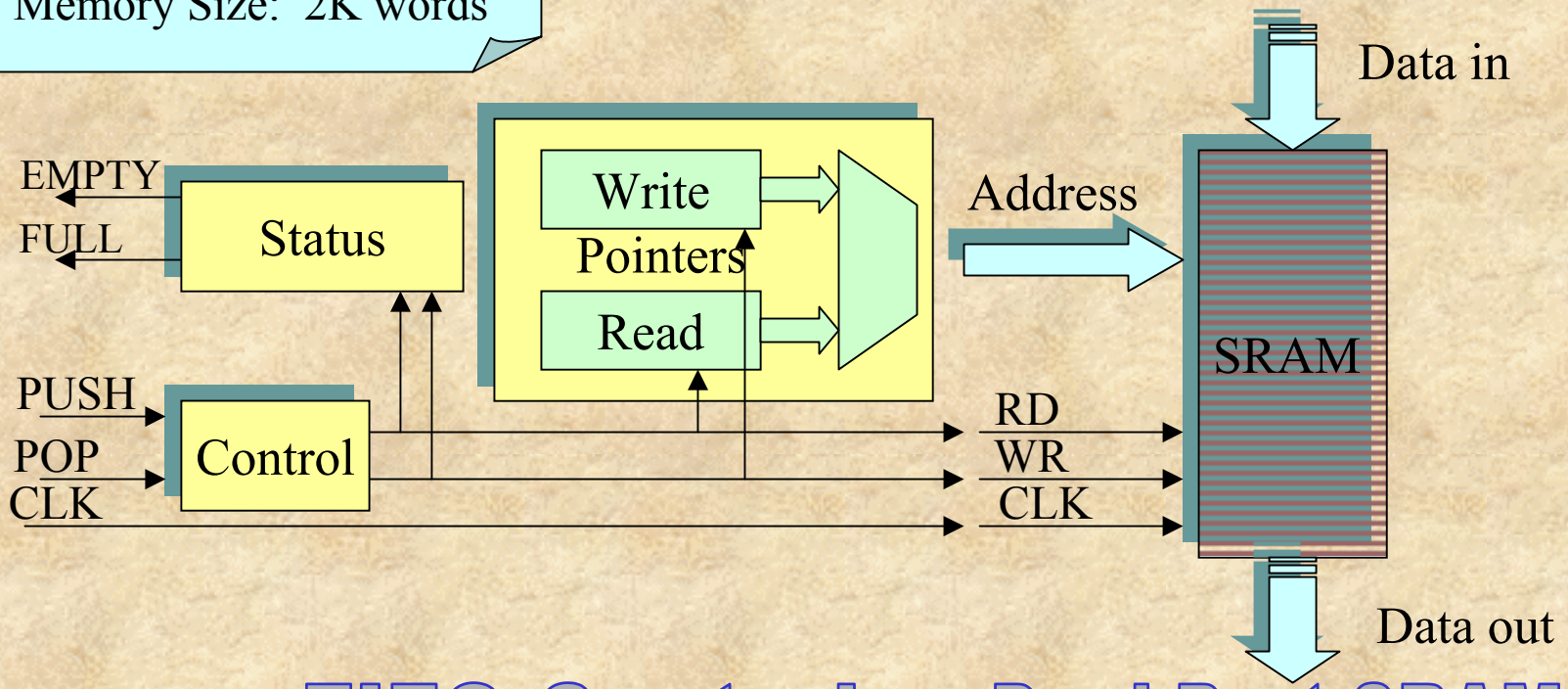


K-chip Block Diagram



FIFO Design

Synchronous FIFO
Operation freq.: 40MHz
Data bus width: 12 bits
Memory Size: 2K words



FIFO Control Dual Port SRAM

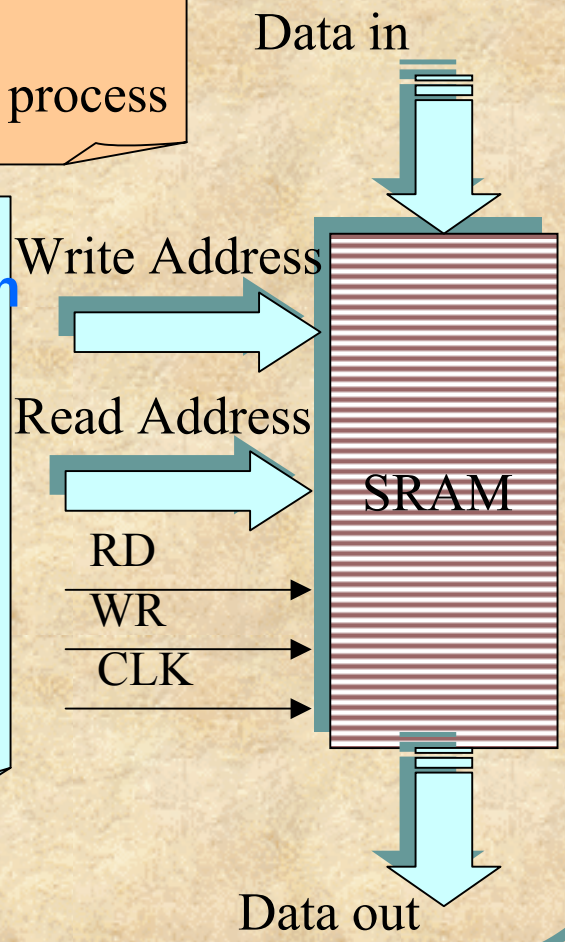
SRAM Features

Radiation Tolerant 0.25μ process

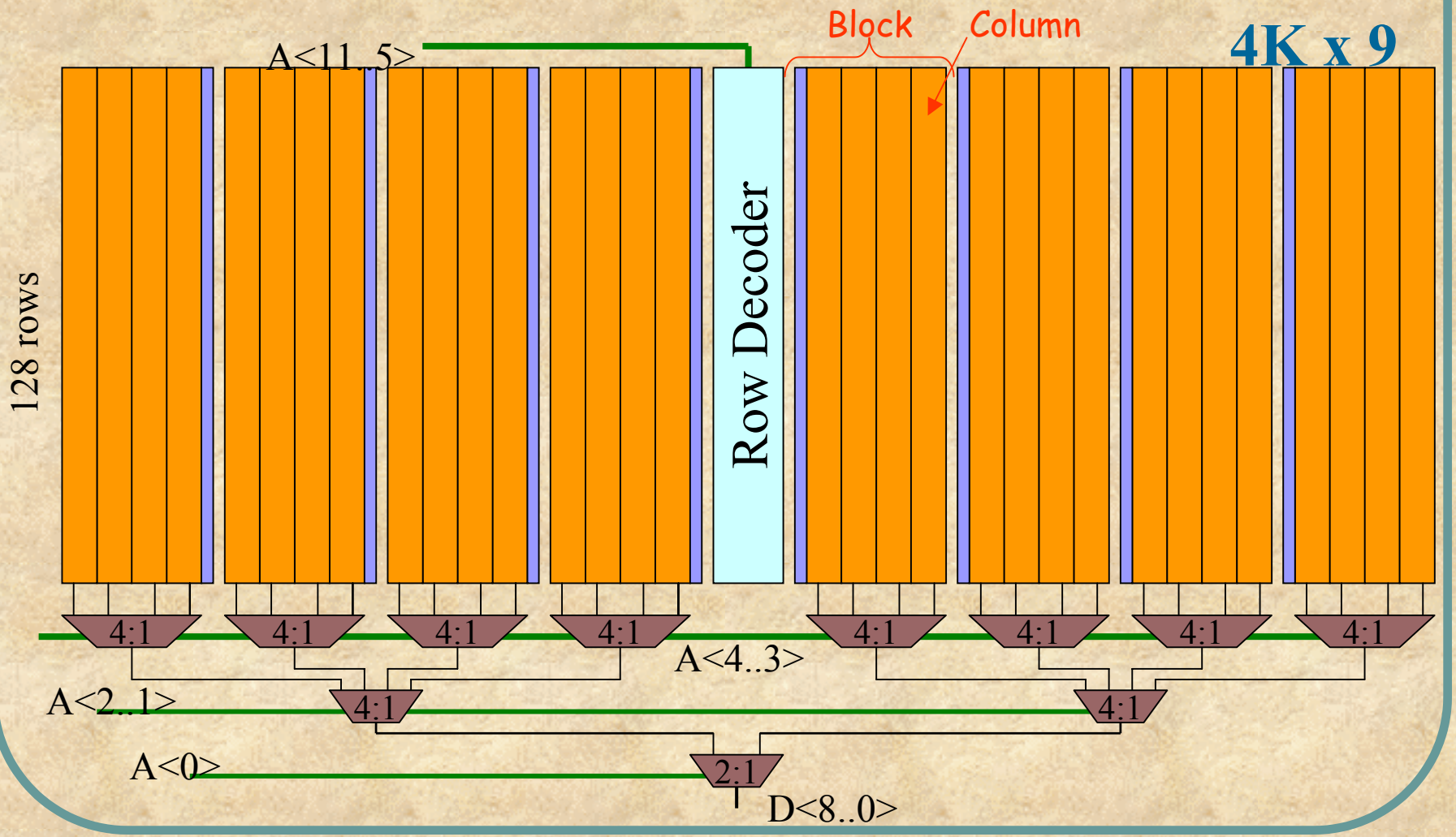
Design Specifications

- Synchronous *pseudo* Dual Port Operation
- Operating frequency: 40MHz
- Flexible configuration of memory size !
- Radiation Tolerant Design

- Data bus width: (n x 9)bits
- Data arrangement: 8 bit + 1 parity bit
- Memory Size: up to 4K words
- Registered Inputs, Latched outputs

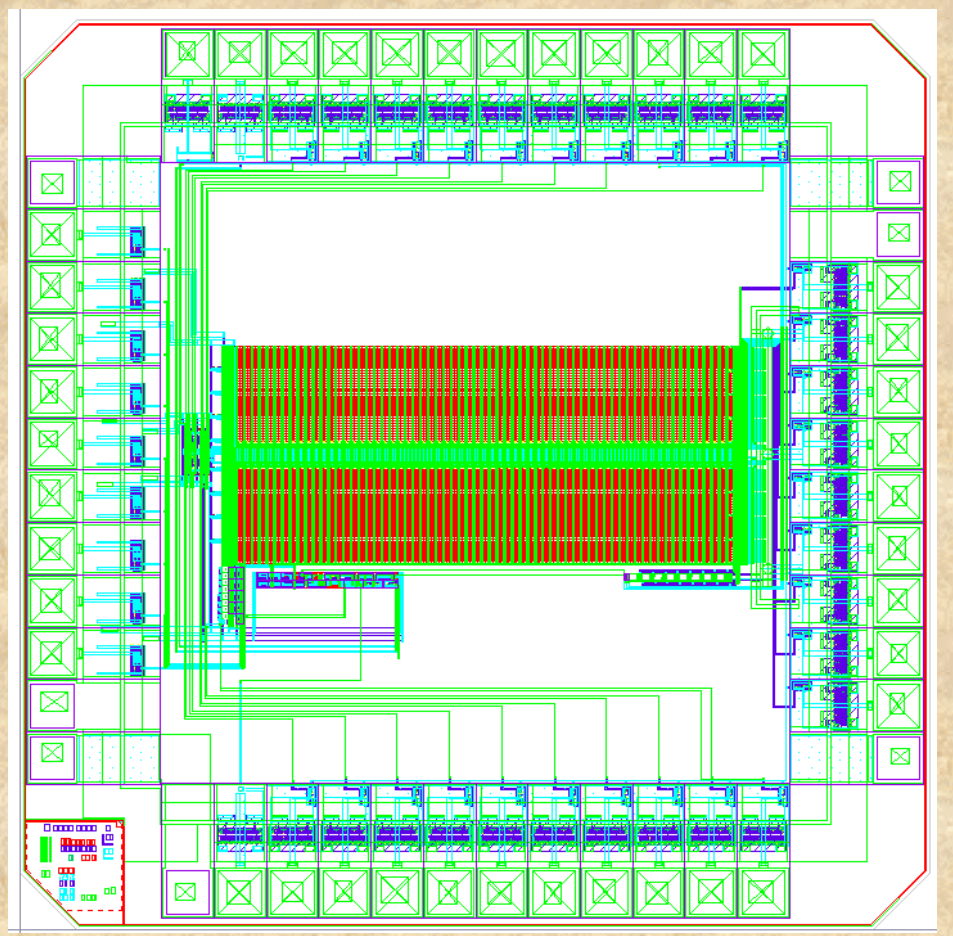


Modular SRAM design.



Submitted SRAM Chips

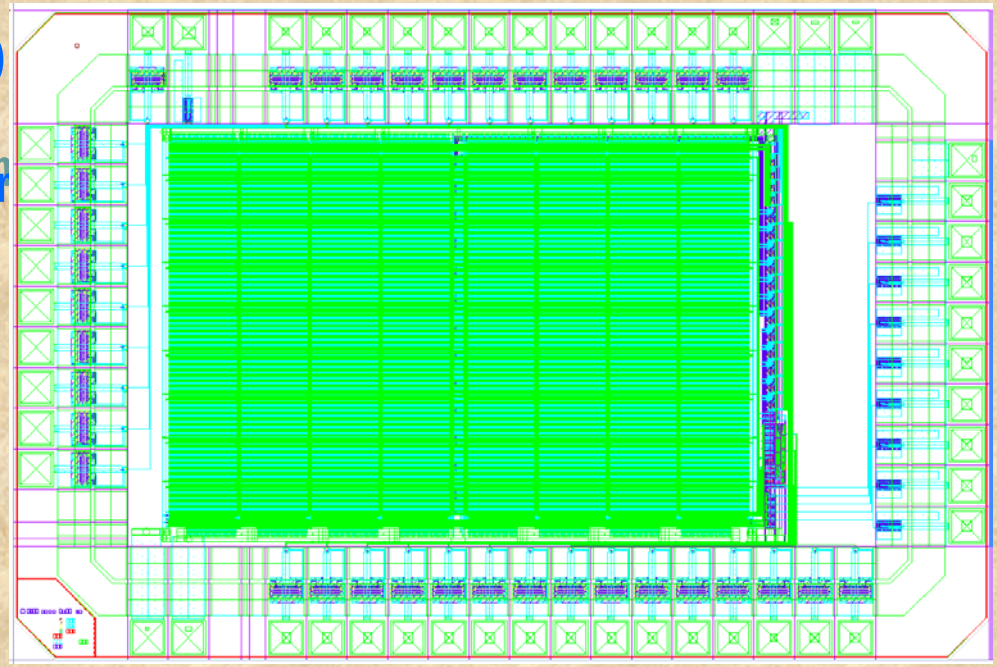
- 1st Prototype (CERN MPW 4)
- Configuration: 1Kx9 bit
- Size: ~560μm x 1,300μm
- Area: ~0.73mm²
- Submitted: Oct. 2000.
- Chip Received: Feb 2001
- Tested: Apr. 2001
- Status: O.K.



Design: CERN_SRAM_1K
Designer: Kloukinas Kostas
EP/CME-PS

Submitted SRAM Chips

- 2nd Prototype (CERN MPW 5)
- Configuration: 4Kx9 bit
- Size: ~1,850μm x 1,300μm
- Area: ~2.4mm²
- Submitted: May 2001
- Chip Received: Aug. 2001
- Tested: Oct. 2001
- Status: O.K.

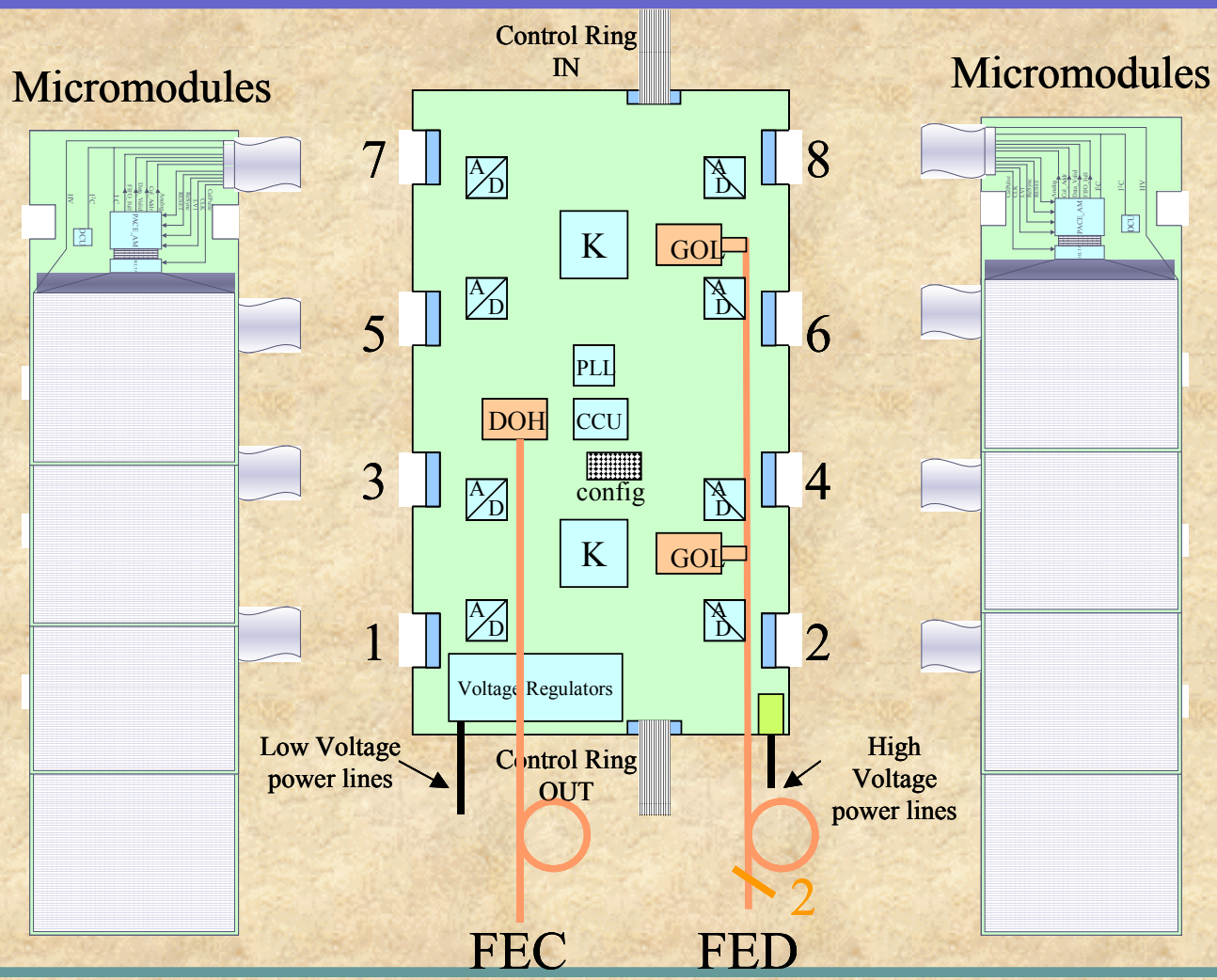


Design: CERN_SRAM_4K
Designer: Kloukinas Kostas
EP/CME-PS

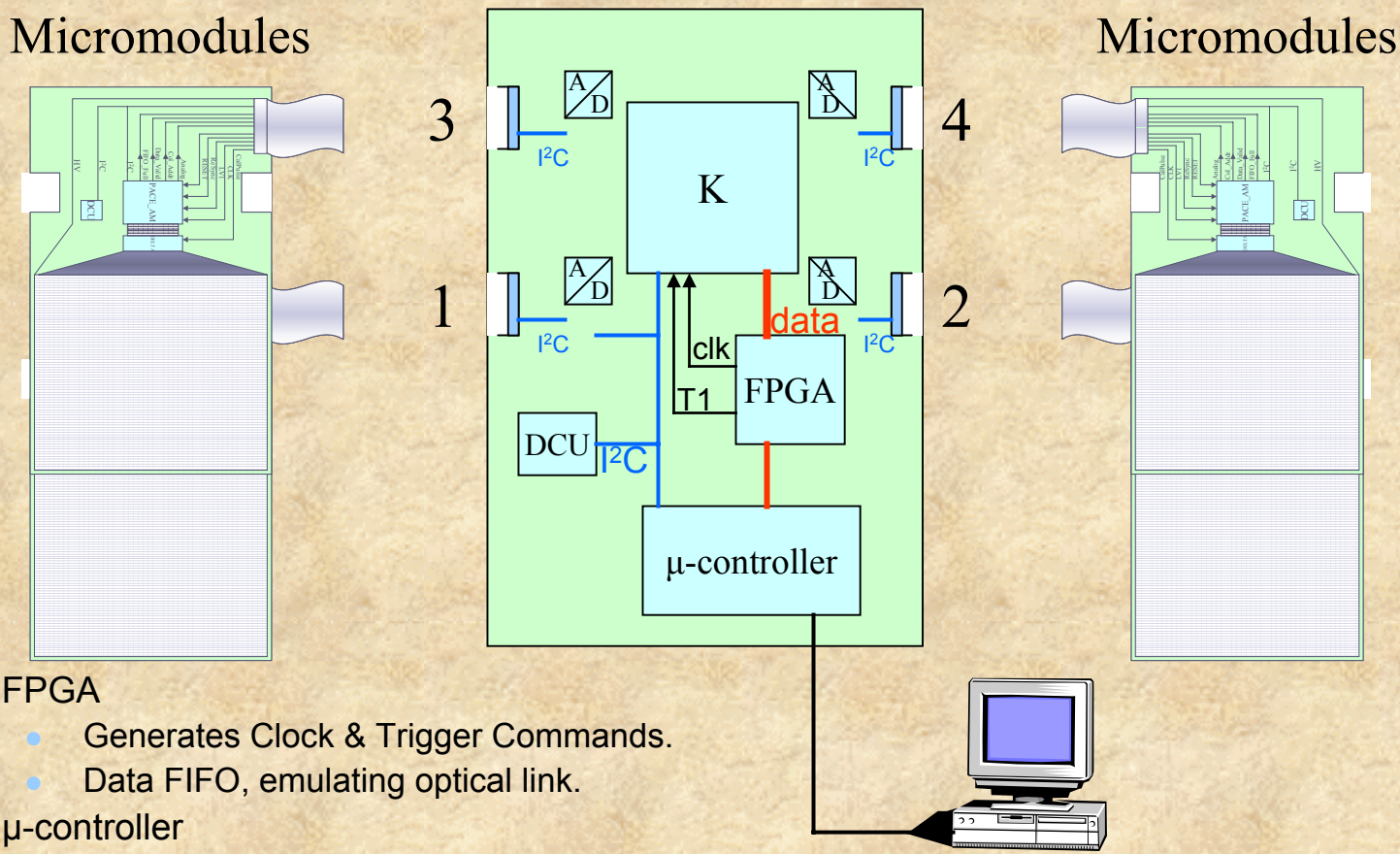
CERN SRAM test results

- Functional tests (4Kx9bit SRAM)
  - Max operating frequency: 60MHz @ 2.5V
  - Read access time: 7.6ns @ 2.5V
  - Power dissipation: 15μW / MHz @ 2.5V for simultaneous R/W access cycles (0.60mW @ 40MHz).
  - Design tested for process variations: -3σ, –1.5σ, typ, +1.5σ, +3σ
- Irradiation tests
  - Total ionizing dose: up to 10MRad
    - No increase in power dissipation.
    - No degradation in performance.
  - Single Event Upsets: under preparation (in collaboration with EP/MIC group)

Final System Motherboard



K-chip Motherboard



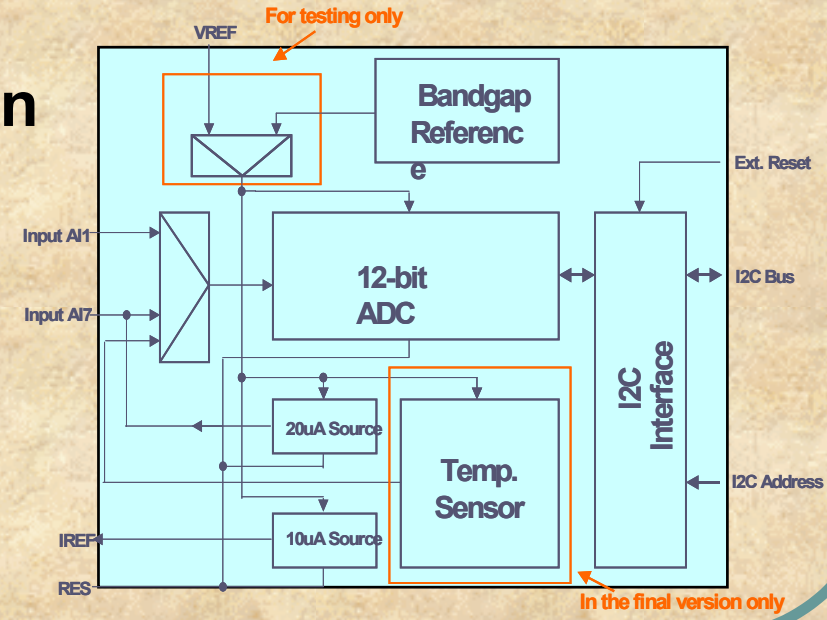
- FPGA
  - Generates Clock & Trigger Commands.
  - Data FIFO, emulating optical link.
- µ-controller
  - I²C master device.
  - Data readout controller.

K-chip Motherboard Scope

- K-chip motherboard
  - Test the functionality of the K-chip.
  - Verify the readout system operation.
    - Proper distribution of the fasts timing signals (clk, Trigger commands) on the motherboard and the μ-module.
  - Test the compatibility of the I2C interfaces of the FE chips (PACE, K-chip, DCU).
  - Test the interfacing between ASICS powered from different supply voltages.
    - PACE & ADC @ 5V, K-chip & DCU @ 2.5V.
  - Evaluate the operation of the DCU chip.

DCU chip evaluation

- **D**etector **C**ontrol **U**nit (CMS Tracker control system)
  - 12-bit ADC, 1ms conversion time
  - 6 analog inputs
  - on-chip temperature sensor (resolution: 0.5^{O}C)
  - I^{2}C interface
- **Investigate possible use in the Preshower Front-End system**
  - Temperature measurement
  - PACE DACs calibration
  - Leakage current measurements



Summary & Future Plans

- K-chip design
  - Data FIFO designed & tested
  - Work in progress on:
    - Digital control logic (PACE readout logic, trigger control, I^2C, etc)
    - 5Volt tolerant pads
    - Differential driver pads for the ADC clock
  - Target submission: CERN MPW 7 (Feb. 2002)
- Motherboard design
  - K-chip motherboard design has started
    - Include as much functionality of the final system as possible.
  - Board expected to be ready in May 2001