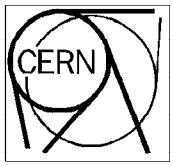

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THE K-CHIP REFERENCE MANUAL

DRAFT

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Please check regularly for updates

Document History

Version 0.1 DRAFT: this is the first draft of the K-chip reference manual.

1 Introduction

This document describes the architecture and the implementation of the K-chip ASIC.

1.1 The K-chip

1.1.1 Functional Description

The K-chip function is to gather data from four PACE chips and format it in a way suitable to be sent over the high-speed digital link. As no data reduction occurs in the front-end system, the K-chip has to cope with the data rates produced by the PACE front-ends; this is detailed in the following sections.

The K-chip receives data in parallel from the PACE chips, builds a packet in a format suitable for the high-speed serial link and sends this to the remote FED cards.

While preparing this data block the K-chip adds some more information to it such as:

- the event number tag
- the bunch counter tag
- CRC information
- error information, if necessary

As the input data comes in 12 bit format, the K-chip aligns the data in contiguous blocks of 16 bits as to maximally utilize the link bandwidth. The data analysis engine in the FED cards will have to unpack the data into 12 bit wide words.

The dataflow used is a simple push type architecture. All K-chips in the system are synchronous and transmit data along their link at the same time, as no data reduction is performed until the FEDs level. Event data prepared in the output buffer of the K-chip are sent to the serial link transmitter. To simplify the system and reduce its cost this link is unidirectional and without flow-control. This means that whenever an error occurs in the transmission medium (either the serializer, the link itself or the receiver) a block of data belonging to one (or potentially even more) event(s) is irremediably lost. As another consequence, the FED has to be able to regain synchronization when one of the K-chips or links is sending data under some error condition.

1.1.2 Block Diagram

A simplified block diagram of the K-chip in the read-out system is shown in

Figure 1-1.

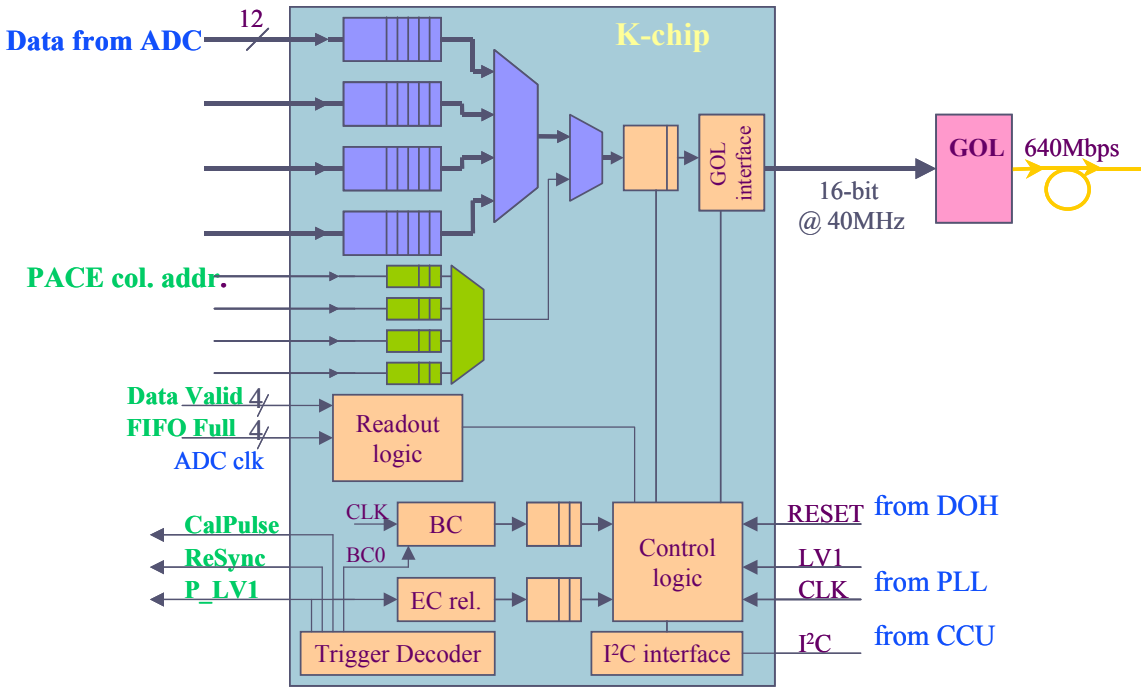

Figure 1-1 K-chip block diagram.

The K-chip consists of the following elements:

- four FIFO buffers, one per input channel. These are 12-bit wide FIFOs and several event deep, see below.
- a multiplexer used to scan the four input FIFOs when a complete event has to be assembled in the output FIFO. This multiplexer also aligns the 12-bit wide data to 16-bit wide format.
- an output buffer, 16-bit wide, where the packet of data corresponding to an event is built before emission to the optical link
- a 16-bit bunch counter used to count continuously the incoming 40MHz clock.
- an 8-bit event counter used to count the number of incoming LV1 triggers.
- a trigger FIFO used to store incoming triggers while the readout of a previous event is in progress
- a control logic to provide the synchronization of the entire ASIC and the supervision of the sequence of operations necessary to build an event in the output buffer.
- a set of user register, accessible through the chip's slow control port (I^2C). The use of these registers are to control and read back status information from the K-chip. They provide also the possibility to the user to write some pseudo-event data into the data FIFOs to test the functionality of the readout chain.

- an I^2C based slow control interface used to access the K-chip internal registers and data FIFOs.

The simplified protocol followed by the K-chip to assemble one event into its output buffer is the following:

- the K-chip monitors continuously the state of its trigger FIFO
- when a trigger is pending in the trigger FIFO, it extracts it together with the bunch counter tag which was stored in it at the moment of the arrival of the trigger signal and stores this in the header of the outgoing data packet in the output FIFO with the K-chip ID number
- the data blocks at the head of the four input FIFOs are read and moved into the output FIFO
- a CRC is computed and appended to the event data packet
- the output is enabled and the packet is streamed out to the serial link.

1.1.3 Operation Modes

The K-chip can be initialized in two modes:

- normal read-out mode
- link test mode

In the first mode, the K-chip assembles event blocks as described above and it used in the normal data acquisition chain. In the link test mode, the K-chip can send out data which can be written into its input FIFOs via the slow control interface. This mode is used essentially as an aid to debug a malfunctioning link outside of the normal data acquisition mode.

1.1.4 Buffer Sizes

The size of the input buffer in the K-chip determines the probability of losing an event (inhibited by the trigger supervisor) because of a momentary congestion of triggers. Using an analytic model of the system we have determined that a buffer of 1.6 Kwords (corresponding to about 13 events) gives an event loss probability of less than 10^{-8}.

The output FIFO only needs to contain one event (~4*148 + overhead = 600 bytes) as no multi-event output buffering is provided.

1.1.5 Error Conditions / Error handling

1.1.6 Link Data Packet Format

Figure 1-2 shows the mechanism that the K-chip employs to rearrange the incoming data in the four input channels.

The format to be used to send data through the High Speed Link is shown in Figure 1-3. Data words are 16-bit wide.

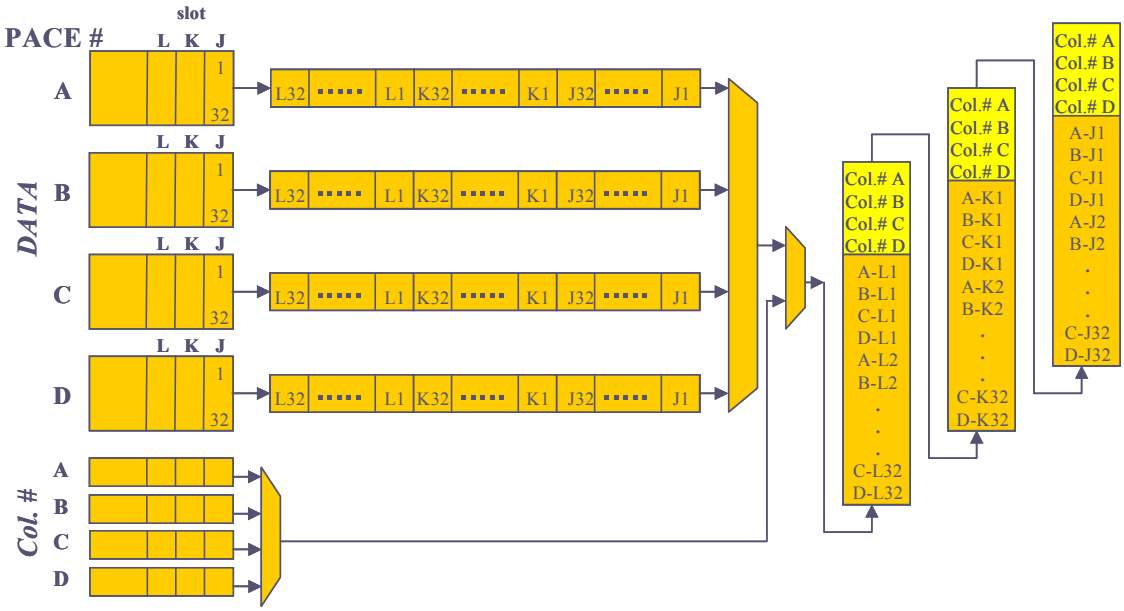

Figure 1-2 Mechanism for the Event Data Formatting.

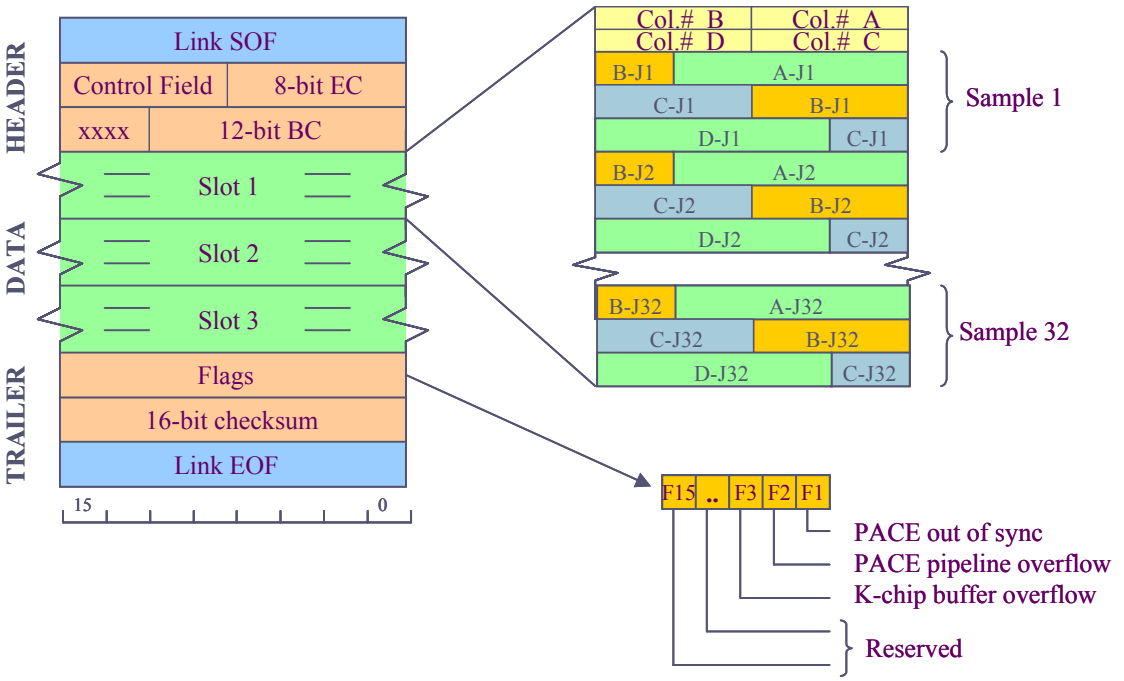

Figure 1-3 Link Data Packet Format.

The Link Data Packet starts with a Header Field followed by the Data Payload and ends with a Trailer Field.

The Header Field consists of:

- a Start Of Frame (SOF) word which is used to synchronize the readout operation
- a Control Field of 8-bits for signaling the type of Data Packet
- an 8-bit Event Counter (EC)
- a 12-bit Bunch Counter (BC)

The Data Payload Field consists of 3 identical data packets each containing information coming from a time slot. Each time slot data packet contains:

- the column addresses of the 4 PACE chips
- the 12-bit digitized values of the 36 data samples contained in one PACE column.

The Trailer Field consists of:

- A 16-bit word containing status flags
- A 16-bit Cyclic Redundancy Checksum word as calculated over the whole information in the data packet except the SOF and EOF words. The CRC field is calculated following the CRC-16 algorithm.
- An End Of Frame (EOF) word, which is used to signal the end of the data packet.

The size of one slot in the Data Packet can be calculated as follows:

(4 PACEs x 36 samples x 12-bit) + 2 words (*column address*) = 1,728 bits or 108 words of 16-bit.

The size of the Data Packet is then calculated as:

3 words (*Header*) + (3 slots x 110 words) + 3 words (*Trailer*) = 337 words.

1.1.7 I^2C Interface

1.1.8 Internal Registers

The Table 1-1 specifies the registers (all 8-bit wide) accessible via the I2C interface in the K-chip (double registers are tagged with a _H-L name).

Table 1-1 K-chip Internal Registers

Name	I^2C Address	Function	Type
CONFIG	0	This register contains various configuration and mode fields as specified below	R/W
ECONFIG	1	This extra-configuration register contains various configuration and mode fields as specified below	R/W
KID	2	K-chip ID register	R/W
Reserved	3		
STATUS	4	This register contains a number of status bits as specified below	RO
FIFOMAP	5	This register contains a pointer to one of the FIFOs in the chip, it is used to direct read/write operations to the corresponding FIFO	R/W
FIFODATA_H-L	6-7	When in Link Test mode, writing to this register causes data to be written into the FIFO pointed to by the FIFOMAP register; a read operation instead reads data from the corresponding FIFO. When in normal mode, read/write operations to this register are ignored	R/W
EVCNT_H-L	8-9	A read operation from this register gives the 16 bit current content of the Event Counter in the K-chip	RO
BNCHCNT_H-L	10-11	A read operation from this register returns the 16 bit bunch counter value used to tag the last event.	RO

1.1.8.1 The *CONFIG* Register

Table 1-2 *Config* register bit assignment.

Name	Position	Function
Mode	7	Determines if the K-chip is in normal or test mode. A 0 in this bit corresponds to normal mode A 1 in this bit corresponds to test mode. The bit is reset to 0 after an external reset to the K-chip.
	6	
	5	
	4	
	3	
	2	
	1	
	0	

1.1.8.2 The ECONFIG Register

Table 1-3 *ECONFIG* register bit assignment,

Name	Position	Function
CLPOS	7	Clear PACE-Out-of-Sequence: when writing a one to this bit, the K-chip clears all the POS bits in the STATUS register. This bit is read always as a 0.
	6	
	5	
	4	
	3	
	2	
	1	
STRSRT	0	Stream read-Out Start. When in Link-Test mode writing a '1' to this bit causes the K-chip to beahve as after having received a T1 signal in input, namely the input FIFOs are transferred to the output FIFO a data are emitted to the link. When in Normal Mode, writing to this bit has no effect.

1.1.8.3 The *STATUS* Register

Table 1-4 *STATUS* register pin assignment.

Name	Position	Function
GERR	7	General error. This is an OR of all error conditions in the K-chip
POS3	6	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 3 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS2	5	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 2 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS1	4	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 1 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
POS0	3	PACE Out-of-Sequence This bit is set when the PACE corresponding to input channel 0 has delivered a column address not equal to the other channels. This bit sticks until the K-chip reset is applied or bit 7 in the ECONFIG is written with a 1.
	2	
	1	
	0	

1.1.8.4 The *FIFOMAP* Register

Table 1-5 *FIFOMAP* bit assignment.

Bits <2:0>	Map
0 0 0	R/W operations to input FIFO channel 0
0 0 1	R/W operations to input FIFO channel 1
0 1 0	R/W operations to input FIFO channel 2
0 1 1	R/W operations to input FIFO channel 3
1 0 0	R/W operations to output FIFO.

1.1.8.5 FIFODATA Register

This 16 bit register is used to write 12 bits of data into the FIFO pointer to by the FIFOMAP register. The write operation actually occurs when the FIFODATA_L register is written. A read operation reads the last in the FIFO and decrements by one the number of words in it.

1.1.8.6 EVNCNT Register

This read-only registers return the value of the Event Counter associated with the last occurrence of a Level 1 trigger

1.1.8.7 BNCHCNT Register

This read-only register returns the value of the Bunch Counter associated with the last occurrence of a Level 1 trigger.

2 Pin Assignments

Table 2-1 Pin assignments sorted by pin functionality.

PIN #	Name	Type	Description
PACE Channel A pins.			
1	A_ADC<0>	5V tolerant input	Channel A ADC data inputs.
2	A_ADC<1>		
3	A_ADC<2>		
4	A_ADC<3>		
5	A_ADC<4>		
6	A_ADC<5>		
7	A_ADC<6>		
8	A_ADC<7>		
9	A_ADC<8>		
10	A_ADC<9>		
11	A_ADC<10>		
12	A_ADC<12>		
13	A_ColAddr	5V tol. input	Channel A Serial Column Address line from PACE.
14	A_DataValid	5V tol. input	Channel A Data Valid line from PACE.
15	A_FIFO_Full	5V tol. input	Channel A FIFO Full flag from PACE.
16	A_PCLK	LVDS output	Channel A 40MHz PACE clock line.
17	A_PCLKb		
18	A_LV1	LVDS output	Channel A PACE First Level Trigger command line.
19	A_LV1b		
20	A_ReSync	LVDS output	Channel A PACE Resynchronization command line.
21	A_ReSyncb		
22	A_CalPulse	LVDS output	Channel A PACE Calibration Pulse Injection command line.
23	A_CalPulseb		
24	A_ADC_CLK	Modified LVDS output	Channel A 20MHz ADC clock line.
25	A_ADC_CLKb		
PACE Channel B pins.			
26	B_ADC<0>	5V tolerant input	Channel B ADC data inputs.
27	B_ADC<1>		
28	B_ADC<2>		
29	B_ADC<3>		
30	B_ADC<4>		
31	B_ADC<5>		
32	B_ADC<6>		
33	B_ADC<7>		
34	B_ADC<8>		
35	B_ADC<9>		
36	B_ADC<10>		
37	B_ADC<12>		
38	B_ColAddr	5V tol. input	Channel B Serial Column Address line from PACE.
39	B_DataValid	5V tol. input	Channel B Data Valid line from PACE.
40	B_FIFO_Full	5V tol. input	Channel B FIFO Full flag from PACE.
41	B_PCLK	LVDS output	Channel B 40MHz PACE clock line.
42	B_PCLKb		

43	B_LV1	LVDS output	Channel B PACE First Level Trigger command line.
44	B_LV1b		
45	B_ReSync	LVDS output	Channel B PACE Resynchronization command line.
46	B_ReSyncb		
47	B_CalPulse	LVDS output	Channel B PACE Calibration Pulse Injection command line.
48	B_CalPulseb		
49	B_ADC_CLK	Modified LVDS output	Channel B 20MHz ADC clock line.
50	B_ADC_CLKb		
PACE Channel C pins.			
51	C_ADC<0>	5V tolerant input	Channel C ADC data inputs.
52	C_ADC<1>		
53	C_ADC<2>		
54	C_ADC<3>		
55	C_ADC<4>		
56	C_ADC<5>		
57	C_ADC<6>		
58	C_ADC<7>		
59	C_ADC<8>		
60	C_ADC<9>		
61	C_ADC<10>		
62	C_ADC<12>		
63	C_ColAddr	5V tol. input	Channel C Serial Column Address line from PACE.
64	C_DataValid	5V tol. input	Channel C Data Valid line from PACE.
65	C_FIFO_Full	5V tol. input	Channel C FIFO Full flag from PACE.
66	C_PCLK	LVDS output	Channel C 40MHz PACE clock line.
67	C_PCLKb		
68	C_LV1	LVDS output	Channel C PACE First Level Trigger command line.
69	C_LV1b		
70	C_ReSync	LVDS output	Channel C PACE Resynchronization command line.
71	C_ReSyncb		
72	C_CalPulse	LVDS output	Channel C PACE Calibration Pulse Injection command line.
73	C_CalPulseb		
74	C_ADC_CLK	Modified LVDS output	Channel C 20MHz ADC clock line.
75	C_ADC_CLKb		
PACE Channel D pins.			
76	D_ADC<0>	5V tolerant input	Channel D ADC data inputs.
77	D_ADC<1>		
78	D_ADC<2>		
79	D_ADC<3>		
80	D_ADC<4>		
81	D_ADC<5>		
82	D_ADC<6>		
83	D_ADC<7>		
84	D_ADC<8>		
85	D_ADC<9>		
86	D_ADC<10>		
87	D_ADC<12>		
88	D_ColAddr	5V tol. input	Channel D Serial Column Address line from PACE.
89	D_DataValid	5V tol. input	Channel D Data Valid line from PACE.
90	D_FIFO_Full	5V tol. input	Channel D FIFO Full flag from PACE.
91	D_PCLK	LVDS output	Channel D 40MHz PACE clock line.

92	D_PCLKb		
93	D_LV1	LVDS output	Channel D PACE First Level Trigger command line.
94	D_LV1b		
95	D_ReSync	LVDS output	Channel D PACE Resynchronization command line.
96	D_ReSyncb		
97	D_CalPulse	LVDS output	Channel D PACE Calibration Pulse Injection command line.
98	D_CalPulseb		
99	D_ADC_CLK	Modified LVDS output	Channel D 20MHz ADC clock line.
100	D_ADC_CLKb		
Gigabit Optical Link interface			
101	TX_Data<15>	2.5V output	Gigabit Optical Link data output.
102	TX_Data<14>		
103	TX_Data<13>		
104	TX_Data<12>		
105	TX_Data<11>		
106	TX_Data<10>		
107	TX_Data<9>		
108	TX_Data<8>		
109	TX_Data<7>		
110	TX_Data<6>		
111	TX_Data<5>		
112	TX_Data<4>		
113	TX_Data<3>		
114	TX_Data<2>		
115	TX_Data<1>		
116	TX_Data<0>		
117	Flag<1>	2.5V output	Flag bits (G-Link mode only)
118	Flag<0>		
119	CAV/TX_ER	2.5V output	Control Available / Transmit Error
120	DAV/TX_EN	2.5V output	Data Available / Transmit Enable
121	Force_FF	2.5V output	Force FF1/FF0 symbols (G-Link mode only)
122	Ready	2.5V input	Data Link Ready
I2C interface			
123	I2C_SCL	2.5V input	I2C interface clock line.
124	I2C_SDA	2.5V bidirectional	I2C interface data line.
125	I2C_Addr<3>	2.5V input	I2C device address.
126	I2C_Addr<2>		
127	I2C_Addr<1>		
128	I2C_Addr<0>		
Fast Timing input signals			
129	CLK_IN	LVDS input	40Mhz LHC clock from PLL chip.
130	CLK_INb		
131	LV1_In	LVDS input	LV1 trigger command input from PLL chip.
132	LV1_Inb		
133	RESET	2.5V input	Hardware reset line from optical hybrid.
Power and Ground			
134	VDD_CORE	2.5V	Core power.
135	VDD_CORE		
136	VDD_PERI		I/O pad power.
137	VDD_PERI		
138	VDD_PERI		
139	VDD_PERI		

140	GND_CORE	GND	Core power.
141	GND_CORE		
142	GND_PERI		I/O pad power.
143	GND_PERI		
144	GND_PERI		
145	GND_PERI		

3 Packaging

4 Appendixes

5 Reference Documents