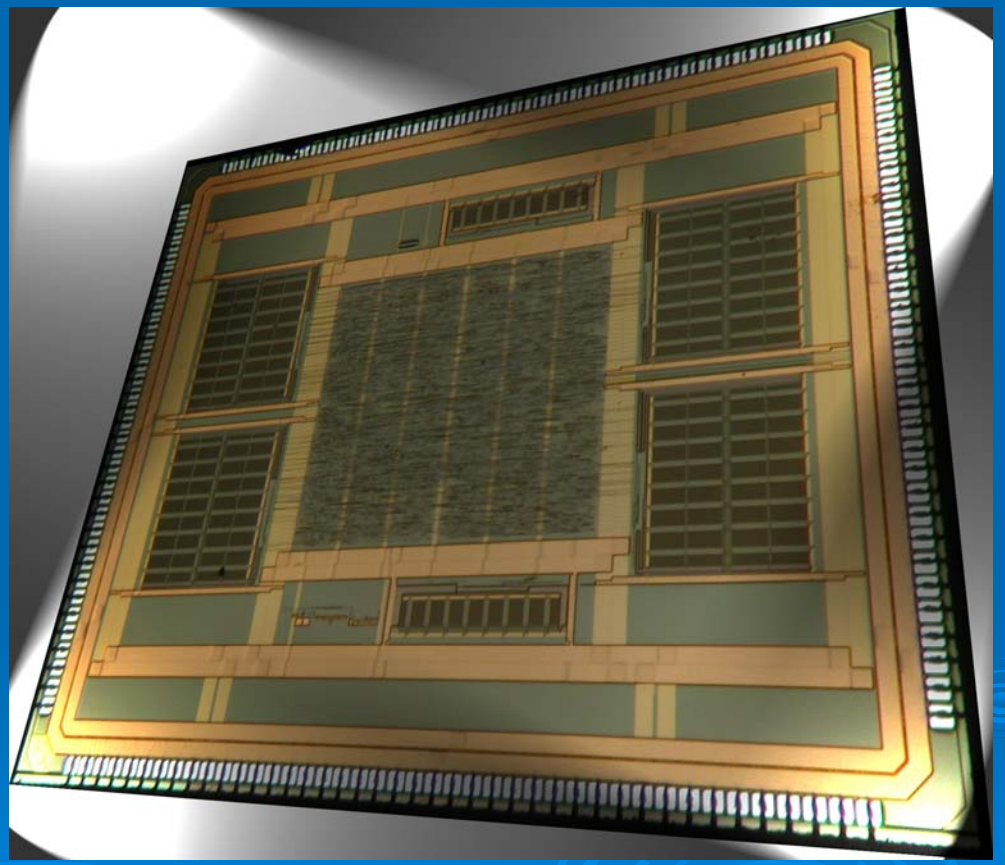
Kchip Design Review
MPW12 submission

Preshower Electronics Meeting

16/10/2003

Kchip

- Test Results
- Changes for MPW12
- Submission Plans
- In System Tests & SEU tests.



Prototype Test Results

- The functionality of the Kchip has been successfully verified.
  - Various data traffic patterns were simulated and test vectors were loaded to the tester for verification.
    - All modes of operation have been verified.
    - No loss of readout synchronization up to 200KHz trigger rate (Poisson distribution).
  - I^2C Interface
    - I^2C interface maximum speed: 3.33 Mbit/s.
    - Kchip has been tested with the CCU chip.
  - All Internal Registers were accessible. ID fuse bits were read out.
  - Calibration Event Generation Logic
    - Verified the Programmable Timing of the CalPulse (on chip DLL)
- A layout bug in the Data FIFO SRAM module has been identified.
  - In specific traffic conditions, some data packets (0.5%) had errors in the data field.

Prototype Test Results

- Maximum operating frequency: 60MHz
  - The limiting factor was due to the bug in the SRAM module.
- Power consumption
  - Test Conditions: 40MHz, VDD=2.5V, T=25^{O}C
  - I_{core} = 68mA, P_{core} = 170mW
  - I_{peri} = 182mA, P_{peri} = 455mW
  - I_{total} = 250mA, P_{total} = 625 mW
- Irradiation Tests
  - Use of an X-ray machine at CERN.
  - Step Irradiation at 1, 3, 5, 10, 20 MRad (SiO_2).
  - Dose Rate = 2.04 MRad/h
    - Devices were operational up to 20 MRad @ 2.5V, 40MHz.

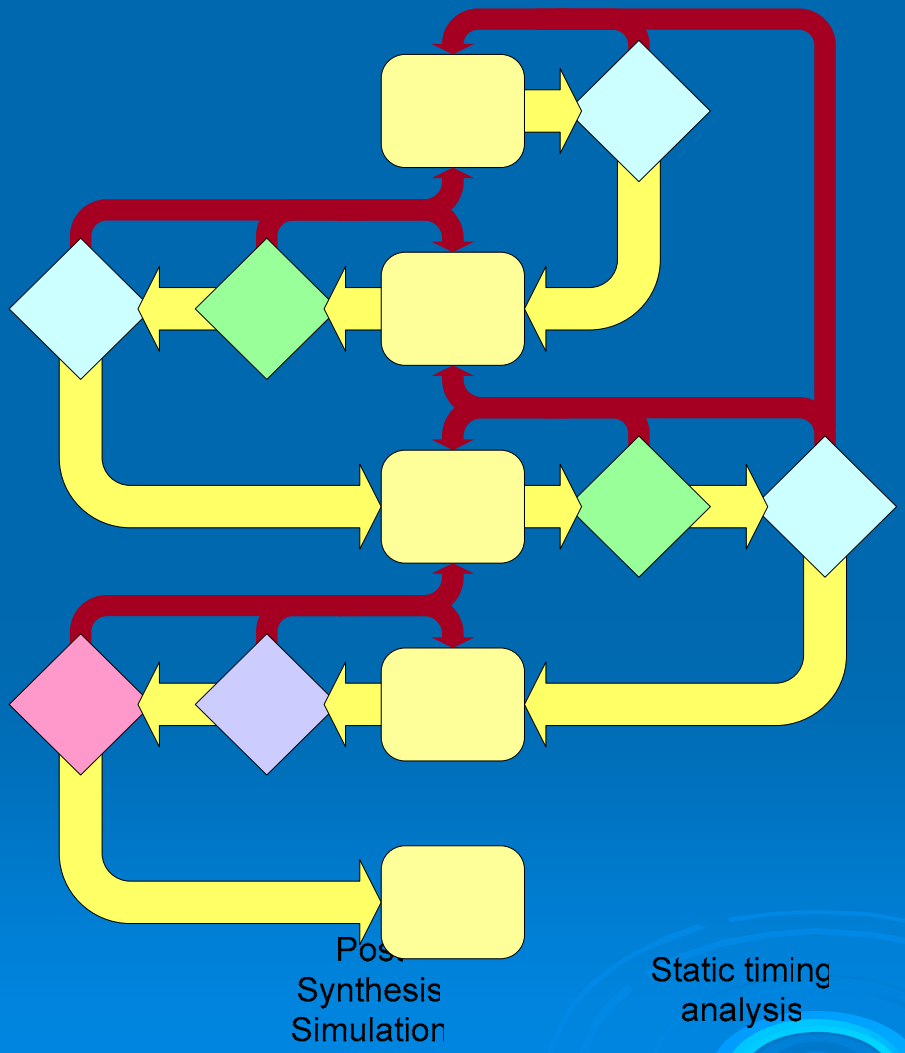
Mandatory Changes

- I^2C I/O pads with hysterisis.
- SRAM bug
  - Layout of the macro cell is modified.
  - Stronger drivers for the SRAM (RA, WA) address buses.
- Configuration Registers Default values
  - CalPulse_WIDTH = 'd2
  - CalPulse_DELAY = 'b11111110
  - ADC pipeline depth ('d6)

Supplementary Changes

- Added Hamming encoding to the SRAMs
  - To decrease SEU rates on SRAMs.
  - Single-error correction and double-error detection.
  - In case of a multiple-error the CRC field is set to FFFFh for that particular packet.
- Added Built-In Self Test to the SRAMs
  - tests all memories in 1.5 ms
    - Tests: all-0s/all-1s, checkerboard, marching-0s, marching-1s.
- Impact on Design
  - Core Logic has expanded by 8%.
  - Total power dissipation will not be affected.

Kchip Design flow



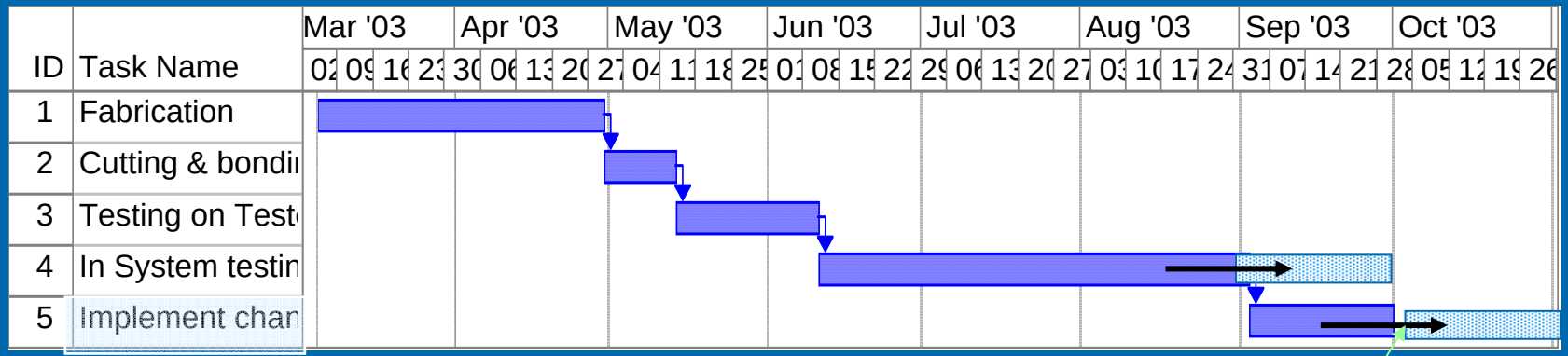
- TO DO:
  - Re-synthesize the core logic.
  - Place & Route.
  - Post Layout simulations and Static Timing Analysis.
  - Final Checks (DRC, LVS).
  - Tape Out. (middle of November).
- Design flow is “scripted”.

Plans for In-System tests

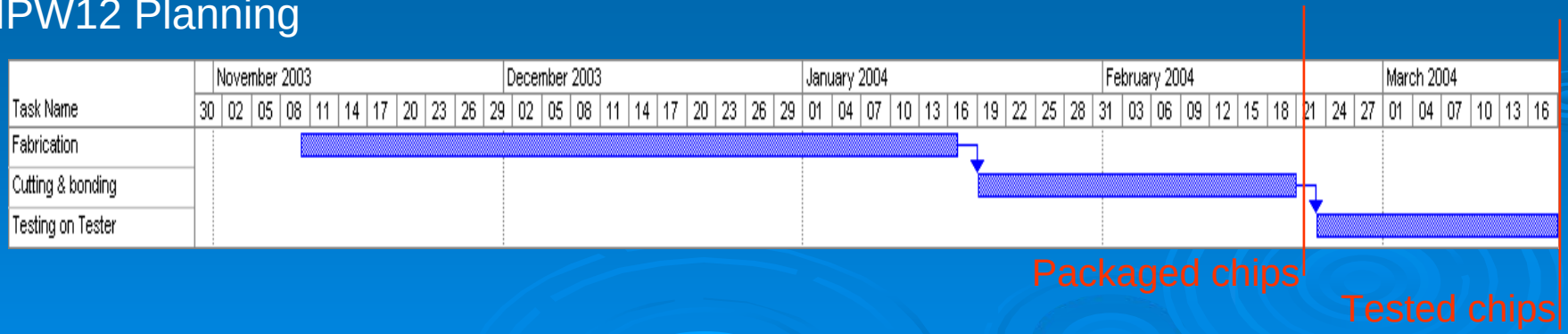
- fpBGA packaged chips have arrived. (144 chips)
  - Unreasonably long delay (~2 months)
- Tester board for fpBGA is currently being assembled.
  - We need
    - To debug the board.
    - Prepare test vector sets.
    - Test a number of chips.
- Integration of the Kchip on the “Preshower motherboard”
    - Verify the Kchip interfacing with the PACE_AM, ADC and control (QPLL, TPLL, CCU) chips.
    - Evaluate the Kchip functionality in the system.
- SEU tests ?
- Unfortunately no feedback before submitting the chip.

Planning

MPW10 Planning



MPW12 Planning



NEWS

- Kchip Design presented on the:
  - 9th Workshop on Electronics for LHC Experiments
    Amsterdam, Sept. 30, 2003

Kchip: A Radiation Tolerant Digital Data Concentrator chip for the CMS Preshower Detector.

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Abstract

The Kchip is a digital chip for the CMS Preshower detector front-end readout electronics. Its primary function is to merge four digital data streams into one and format it in a way suitable to be sent over an optical high speed link. The "Kchip" has been developed on a commercial 0.25 μm CMOS technology using radiation tolerant layout techniques. Special design considerations were also taken in order to protect the operation of the chip against the Single Event Upsets. This paper introduces briefly the front end readout architecture of the CMS Preshower silicon strip detector and presents the design of the Kchip. The experimental test results from the first prototype chip are being reported.

I. Introduction

The front-end readout electronics of the CMS Preshower detector are based on a hybrid architecture consisting of an analog pipeline memory followed by an ADC and a non-zero suppressed digital transmission to the off-detector electronics. Figure 1 shows a general block diagram of this architecture[1].

The signals from the silicon strips are amplified by a 32 channel preamplifier chip, named the "DELTA" chip, and then are sampled at a 40MHz rate and stored in a 32 channel analog pipeline memory chip, named the "PACE-AM" chip. The "DELTA" and "PACE-AM" chips are custom made chips on 0.25μm CMOS technology and compose the "PACE" chipset. Upon the arrival of a trigger signal 3 consecutive columns in the "PACE-AM" memory are blocked and their column addresses are written to a FIFO. A readout cycle then follows that multiplexes out of the "PACE-AM" the analog data at a rate of 20MHz. The data are digitised by a CMOS 0.25μm, quad channel, 12-bit, 40Msps ADC chip [1]. The digitised data are transmitted without any zero suppression to the off-detector electronics through a unidirectional Gigabit Optical Link (GOL) [2]. To utilize more efficiently the bandwidth of the links and reduce the overall number of links needed to readout the entire detector, it is necessary to merge the data streams generated by 4 "PACE" chipsets. This data concentration operation is performed by a custom made chip named the "Kchip".

[1] All the front-end electronics chips in the Preshower detector are made on the same radiation tolerant 0.25μm CMOS commercial available process.

The "Kchip" incorporates all the necessary functionality for reading out the "PACE" chips and format properly the data in order to by transmitted through the gigabit optical links. It monitors the operation of the "PACE" pipeline memories and the readout operation of the "PACE" chips and signals possible erroneous conditions. It also receives the fast timing signals from the "control chips" and distributes them to the "PACEs" and the ADCs.

This paper introduces the design of the "Kchip" and presents experimental test results from the first prototype chip.

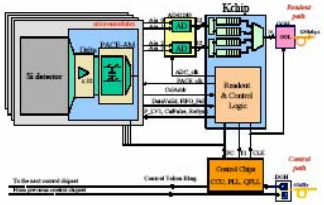

Figure 1The Preshower Front End Readout Architecture.

II. Kchip Architecture

A. Data Path Architecture

The block diagram of the "Kchip" is shown in Figure 2. The chip receives two 12-bit multiplexed data busses from the ADCs using LVDS signalling. The data are passed through a demultiplexing circuit that uses both edges of the system clock to separate the two data streams to four data channels corresponding to the four "PACE" chips. The data are pushed into 4 independent "Data FIFOs". A "PACE controller" circuit generates the sequence for reading out the "PACE" chips as shown in Figure 3. It also deserializes the column address information as transmitted by the "PACE" chips and pushes it into the "Column Address FIFO".

This logic emulates the readout state machine of the "PACE" chip and generates a copy of the control signals that the "Kchip" receives from the "PACE". The "Error Logger" logic compares this set of signals and identifies possible loss