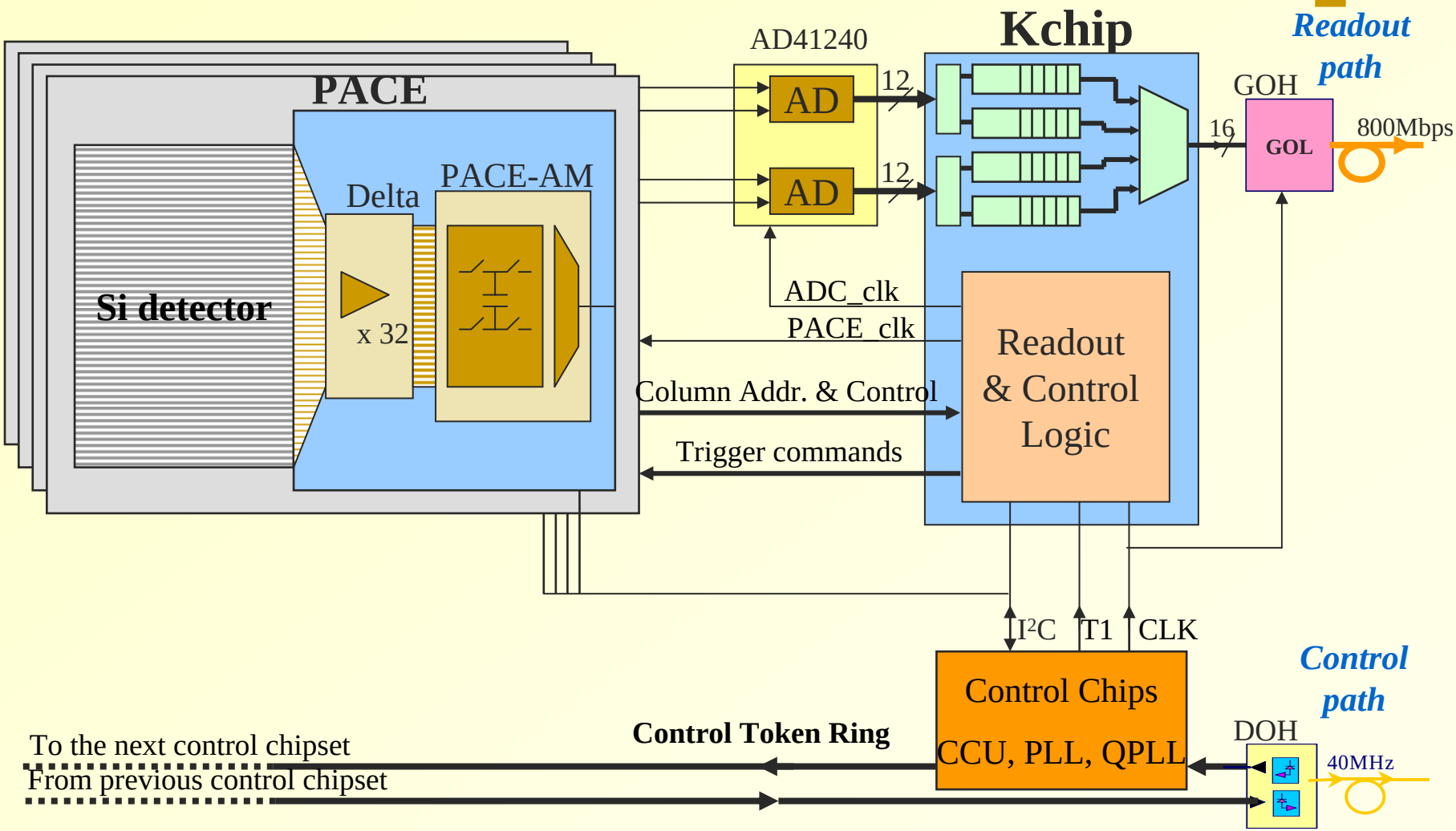
Kchip: A Radiation Tolerant Digital Data Concentrator chip for the CMS Preshower Detector

Preshower ESR

KLOUKINAS Kostas
CERN, EP/CME

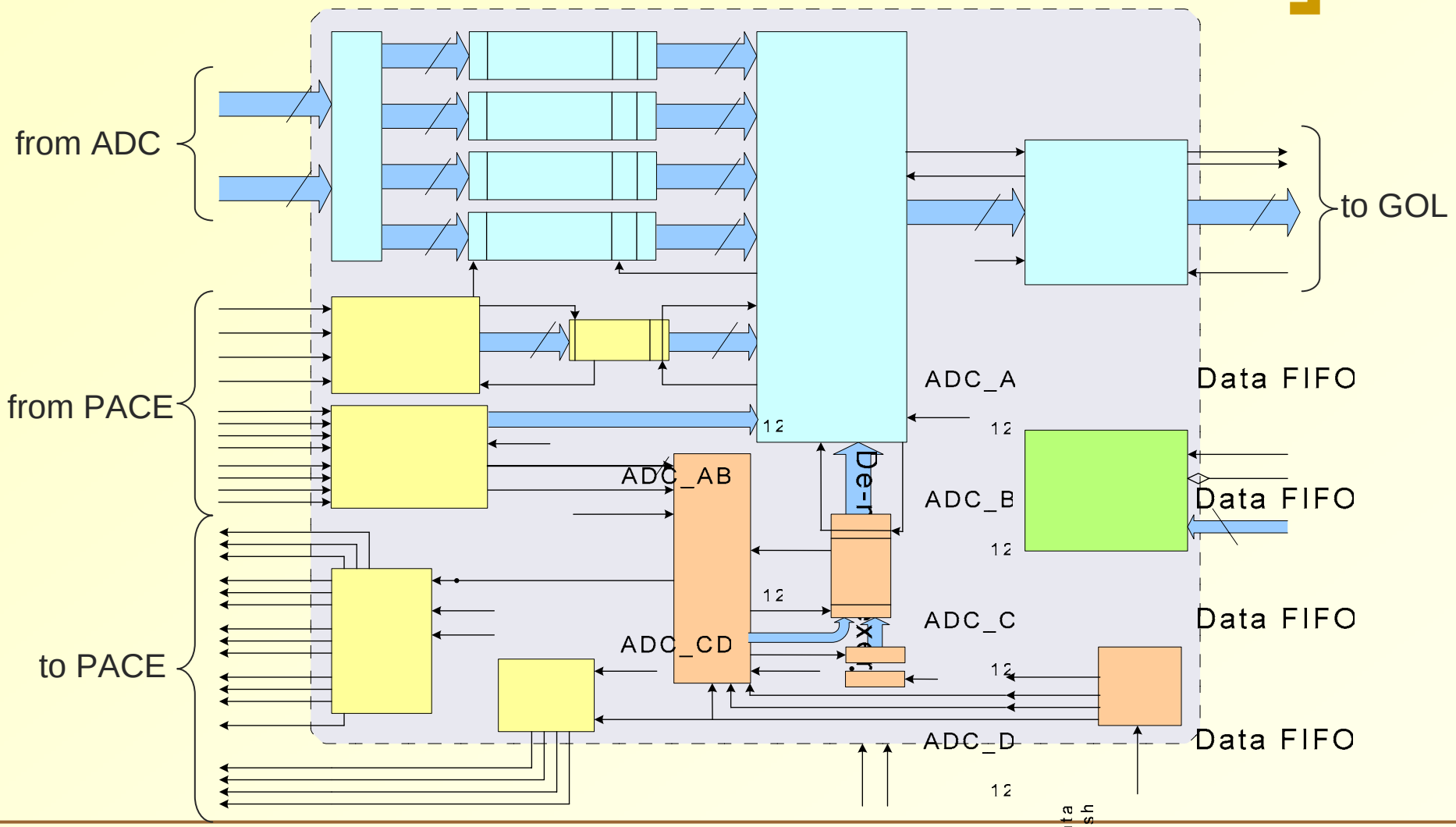
Preshower Front-End Readout



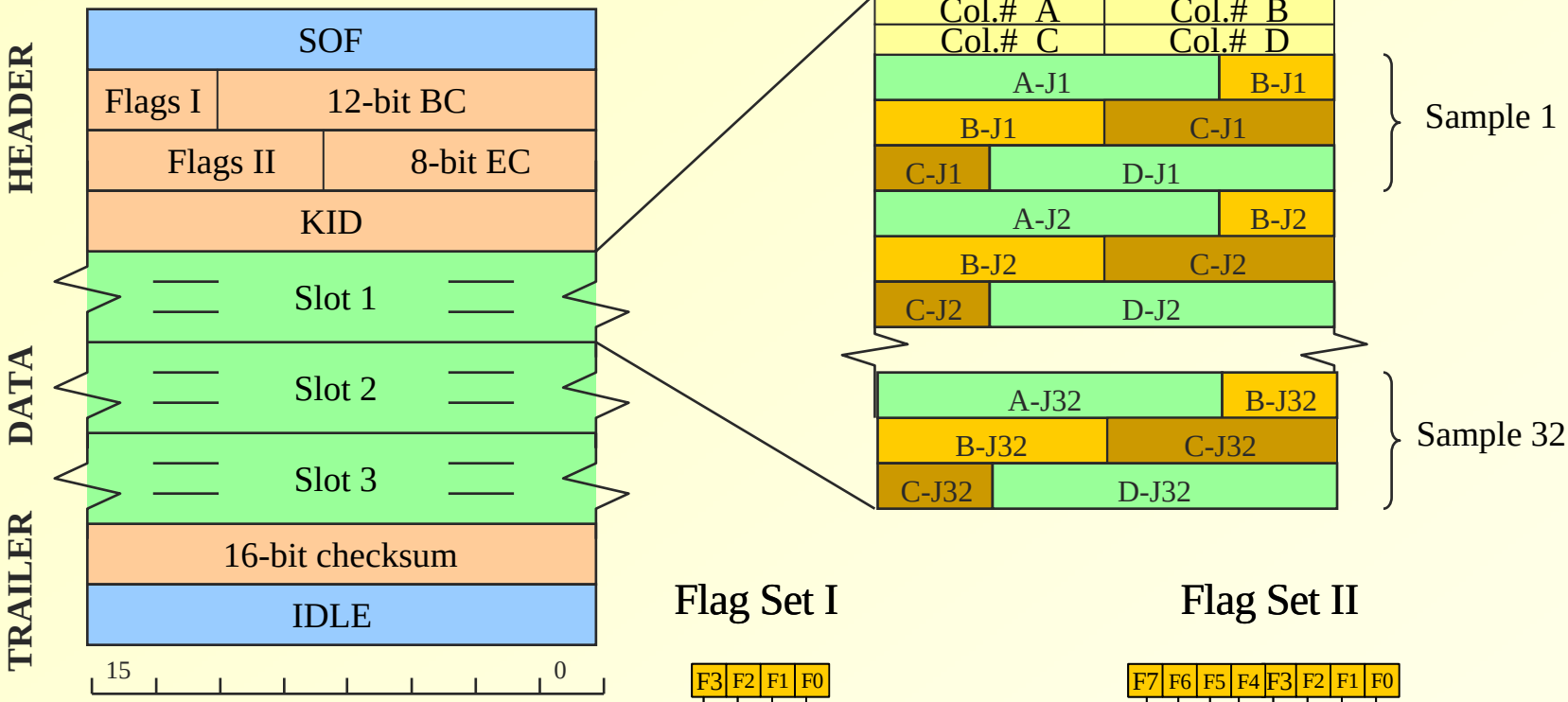
Kchip Functionality

- Data Concentration
  - Can be configured to readout 1~4 PACE chips.
- Event Data Formatting
  - Align data into 16-bit words.
  - Assemble an Event Packet.
  - Assign a Bunch Count (BC) and Event Count (EC) Identifier.
  - Link Protocol for transmission through a Gigabit Optical Link.
- Readout Controller
  - Trigger Command Decoding
  - PACE Readout Synchronization Monitoring
  - Front-End Buffers Overflow Detection / Prevention
  - PACE & ADC clock and Trigger Command Distribution

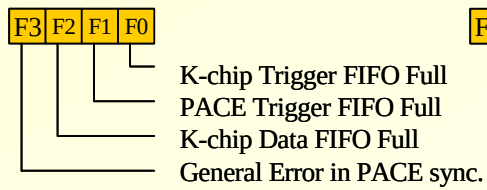
Kchip Block Diagram



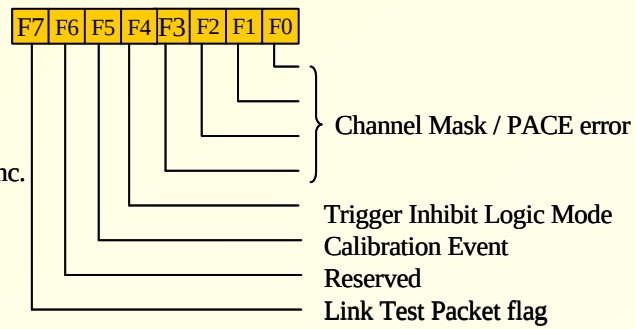
Packet Format



Flag Set I

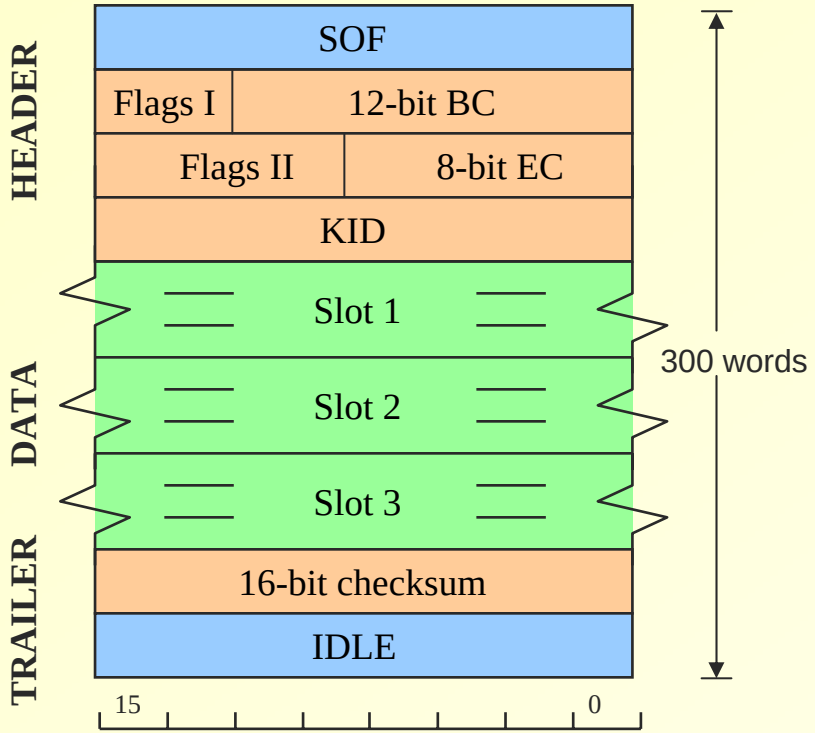


Flag Set II

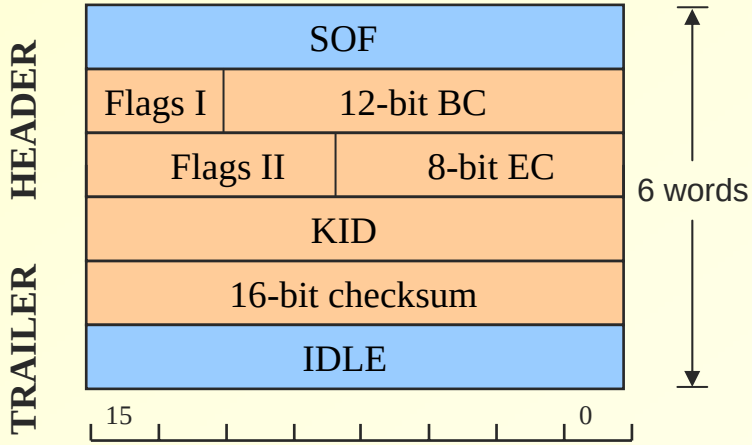


Packet Types

Normal Event



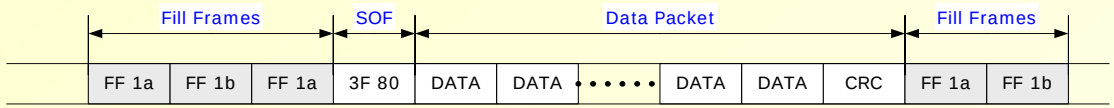
Null Event



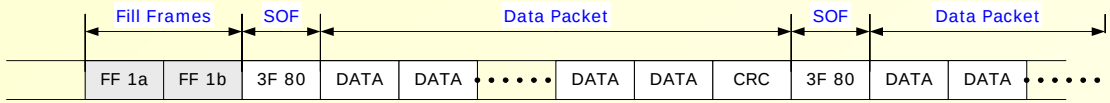
Link Protocol

- The Kchip can seamlessly use both encoding schemes supported by the GOL chip: the CIMT and the 8b/10b encoding.

CIMT encoding

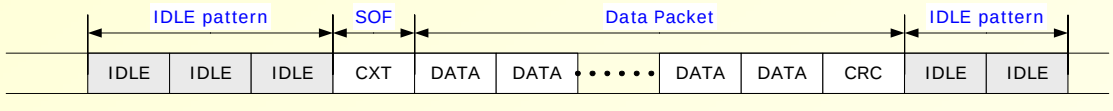


Packet format in CIMT encoding.

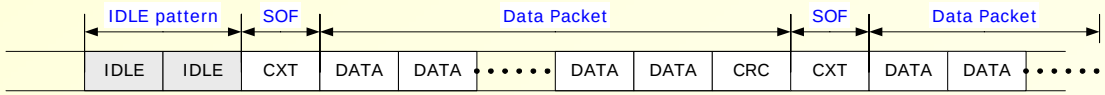


Packet format in CIMT encoding for back-to-back events.

8b/10b encoding



Packet format in 8b/10b encoding.



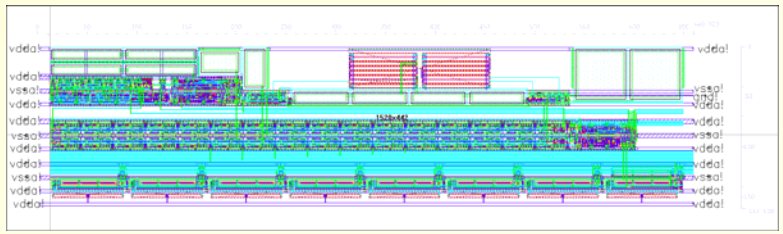
IDLE = <K28.5, D5.6> or <K28.5, D16.2> : Idle
CXT = <K23.7, K23.7> : Carrier Extend

Packet format in 8b/10b encoding for back-to-back events.

Calibration Circuit & DLL

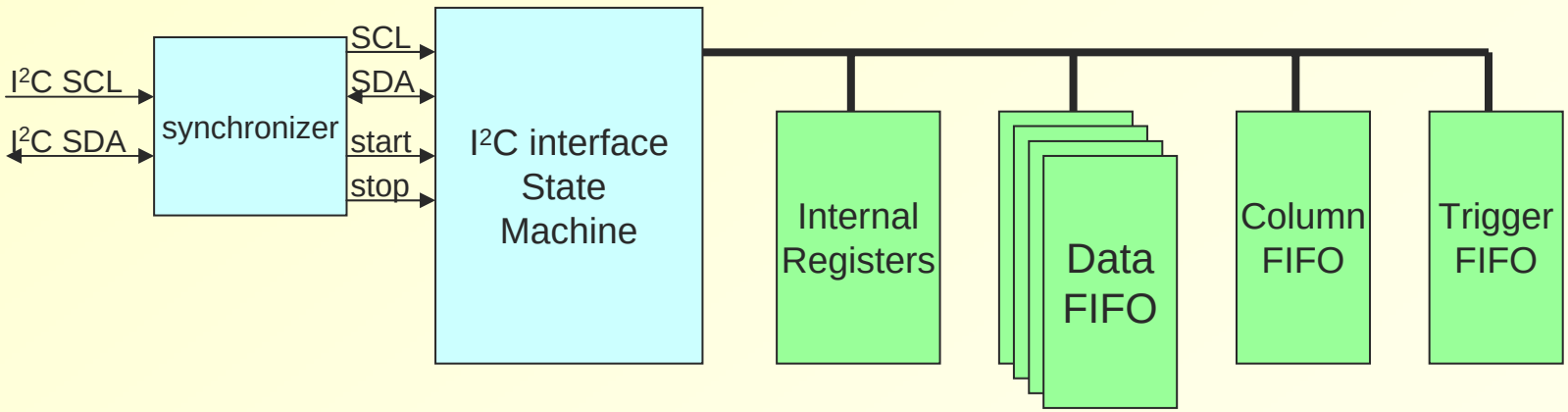
- The Kchip distributes to the PACE chips a calibration pulse of programmable delay with respect to the system clock and with programmable width (1 – 256 cycles).
- The DLL from APV25 chip has been ported into the Kchip.
  - Delay adjustment: 16 steps of 3.25ns
- After an interval equal to the trigger latency a Trigger signal is generated by the Kchip in order to readout the Calibration Data.
  - The automatic generation of the Calibration Event can be disabled.

The DLL block as delivered from RAL.



I²C Interface

- The I²C interface can be used to access:
  - The Kchip Internal Registers
    (There are 25 Status & Control Registers).
  - The Kchip FIFOS (Data, Column Addr. and Trigger FIFOs).
- Supports 7-bit addressing Single Byte transfers.
- Synchronous design. (40MHz system clock)



Buffer Overflow Handling

- The Kchip can detect imminent overflow conditions and prevent buffers from actually overflowing and lose synchronization.

- Trigger Inhibit Logic on Kchip.
  - If a FIFO signals an *Almost Full* condition then the Trigger signal will be gated until some data has been read out and space is made available.
  - The readout chain gets informed about the trigger gating condition and NULL Events are inserted to maintain Event Readout Synchronization.
  - The Trigger Inhibit logic can be enabled or disabled.

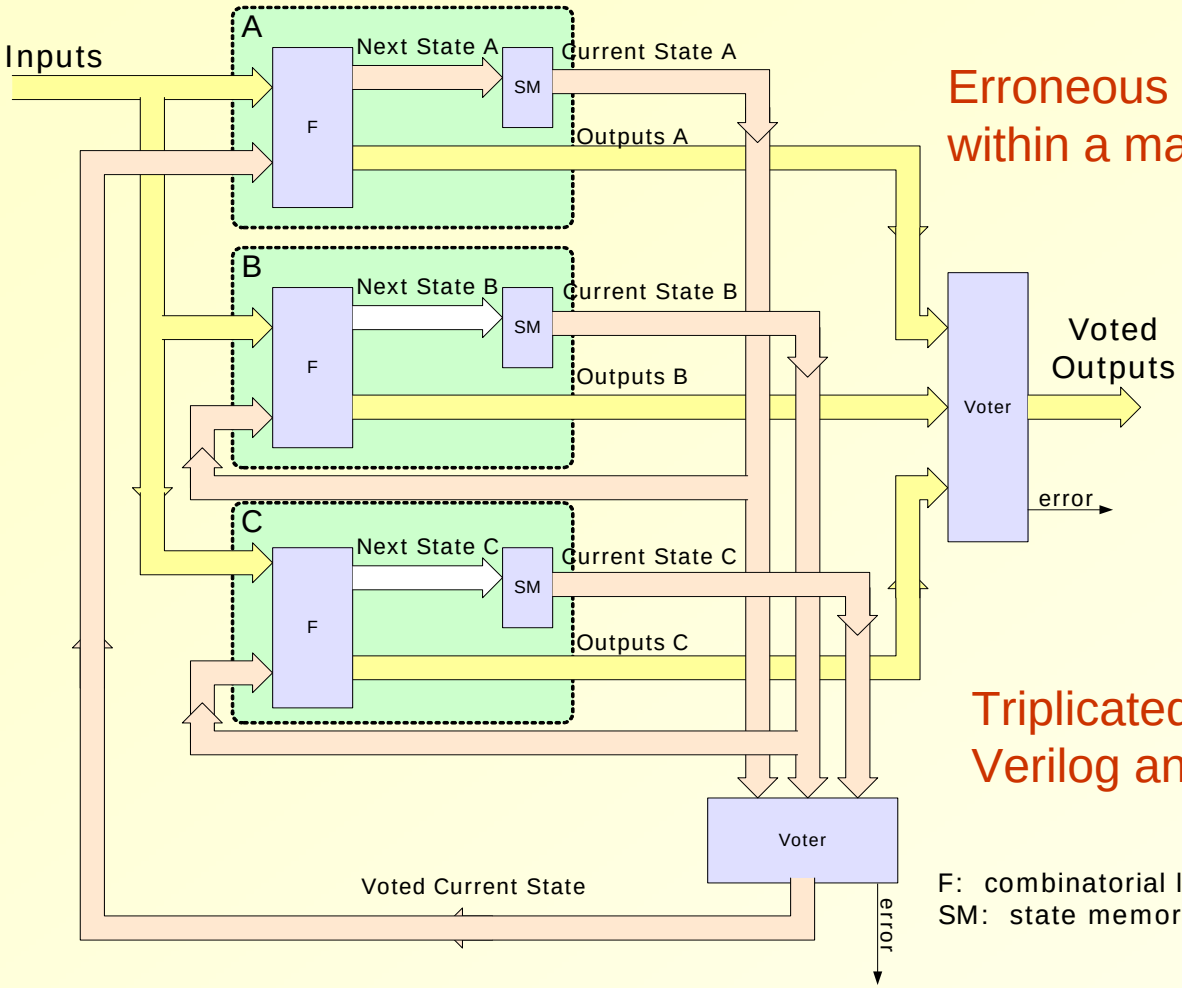
PACE synchronicity monitoring

- Under normal operation the pipeline memories in the PACE chips should run synchronously.
- The Kchip monitors the synchronization of the PACE chips by comparing the status of their control signals on a cycle to cycle basis.
  - Cross-checks the 4 “DataValid” signals.
  - Cross-checks the 4 “AlmostFull” signals.
- “PACE out of sync” condition is signaled when the readout sequence in any of the PACE chips is not synchronous to the Kchip internal readout sequencer.
- The “PACE out of sync” condition is flagged in the data packet header and in a special status register accessible through the I^2C bus.

Implementation Issues

- SEU Tolerant Design
  - Protect Control Logic using Triple Module Redundancy.
    - All State Machines and Configuration Registers have been triplicated.
  - Minimal protection of the Data Path.
    - SEU errors affect the integrity of small amount of information and does not lead to a loss of readout synchronization.

Triplicated State Machine



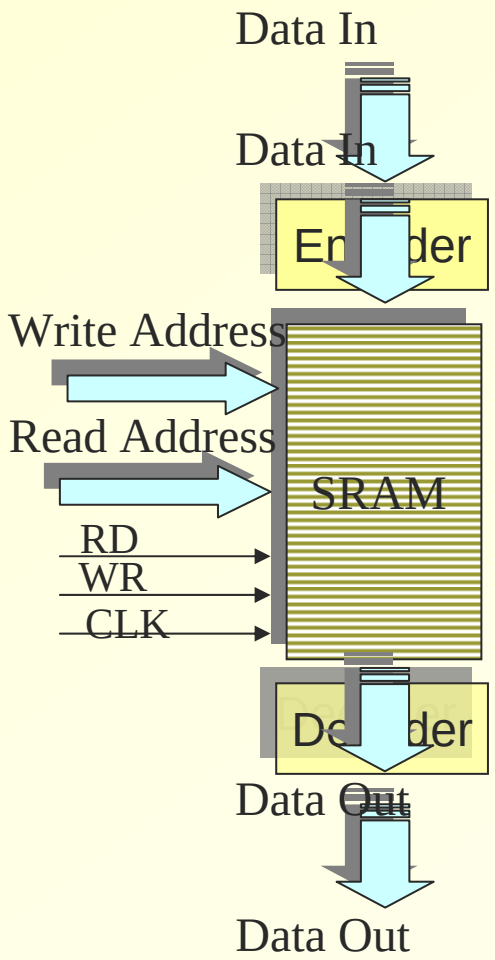
Erroneous state machine will recover within a maximum of 3 clock cycles.

Triplicated logic was described in Verilog and has been synthesized.

F: combinatorial logic
SM: state memory

Hamming Encoding

- Data spent most of their time waiting in the FIFOs.
  - Protect SRAM against SEUs.
- Use Hamming encoding to protect the contents of the FIFOs.
  - Capability:
    - Correct **single errors** in the same word.
    - Detect **double errors** in the same word and flag the data packet.
      - In case of a multiple-error the CRC field is set to FFFFh for that particular packet.



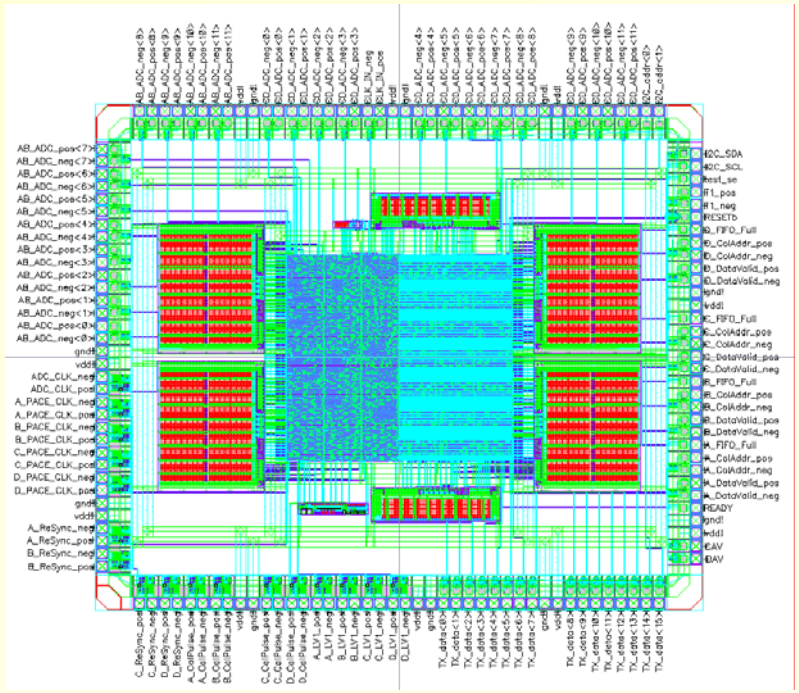
Design For Testability (DFT)

- SRAM testing
  - In Kchip V3a the SRAMs can be tested through the I^2C bus.
  - Kchip V3b has a Built In Self Test (BIST) for all SRAMs
    - Initiate testing with an I^2C command.
    - Test all memories in 1.5 ms
    - Tests: all-0s/all-1s, checkerboard, marching-0s, marching-1s.
- Scan Path
  - Kchip V3a has 1 scan path
    - Test time ~ 6min.
  - Kchip V3b has 4 scan paths that run in parallel.
    - Test time ~ 1min.
  - Use Automatic Test Pattern Generator (ATPG).

The Synthesized Chip

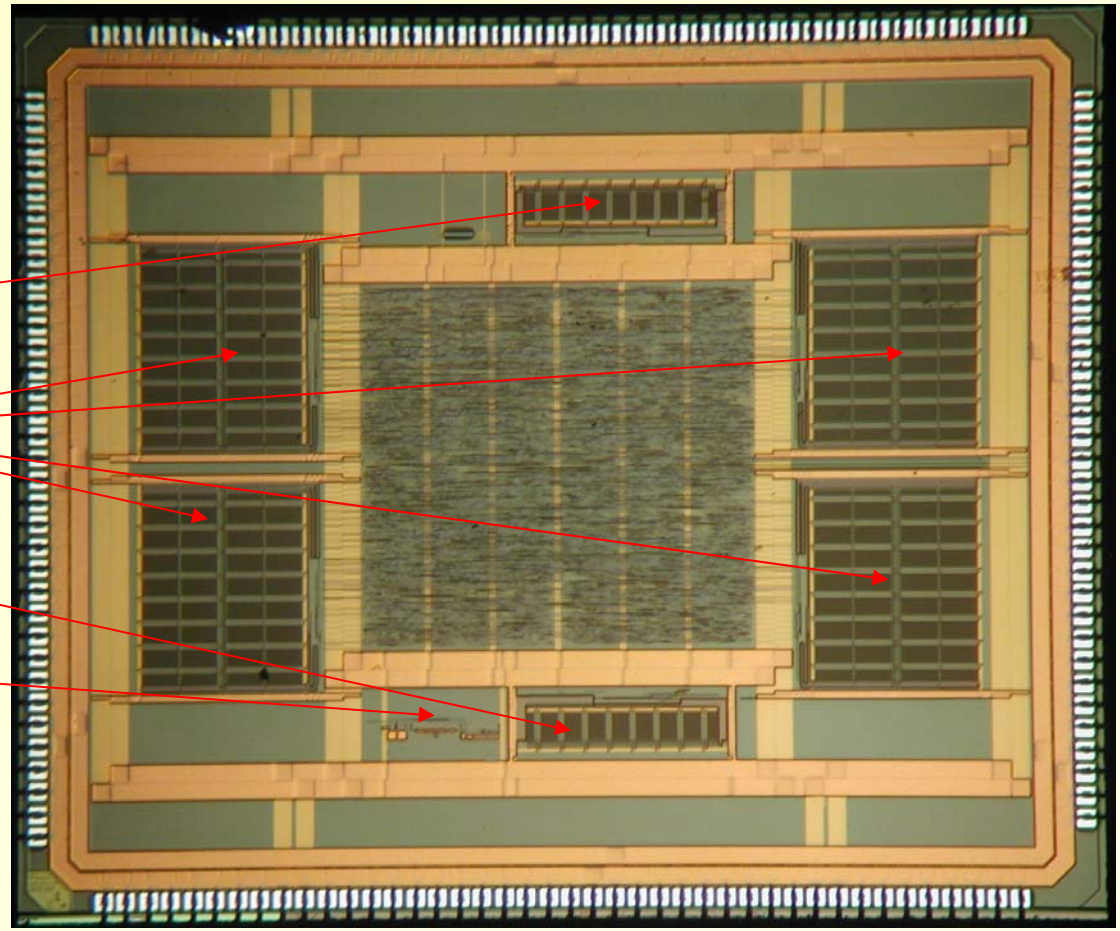
- Number of Digital Standard cells
  - Registers: 1,400
  - Gates: 13,300
- Clock tree statistics
  - Number of buffers: 189
  - Number of Levels: 6
  - Max. delay: 685 ns
  - Max. skew: 65 ps
- Special Macro Cells
  - 4x 1024 x 18bit, dual-port SRAM
  - 2x 128 x 27bit, dual-port SRAM
  - DLL
- Number of pad cells
  - I/O pins: 131
  - Power pins: 17
  - Total pins: 148

Size: 6 x 5 mm²
Pad Limited design.



Kchip Layout

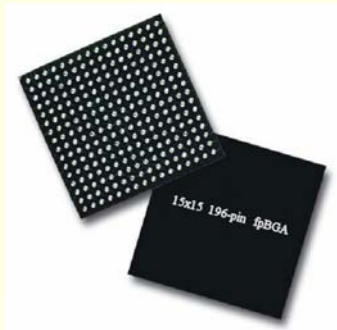
1st Prototype
CERN MPW10
Submitted: Feb. 2003
Received: June 2003



Kchip designers:
Kostas Kloukinas, CERN EP/CME
Sandro Bonacini, CERN EP/MIC

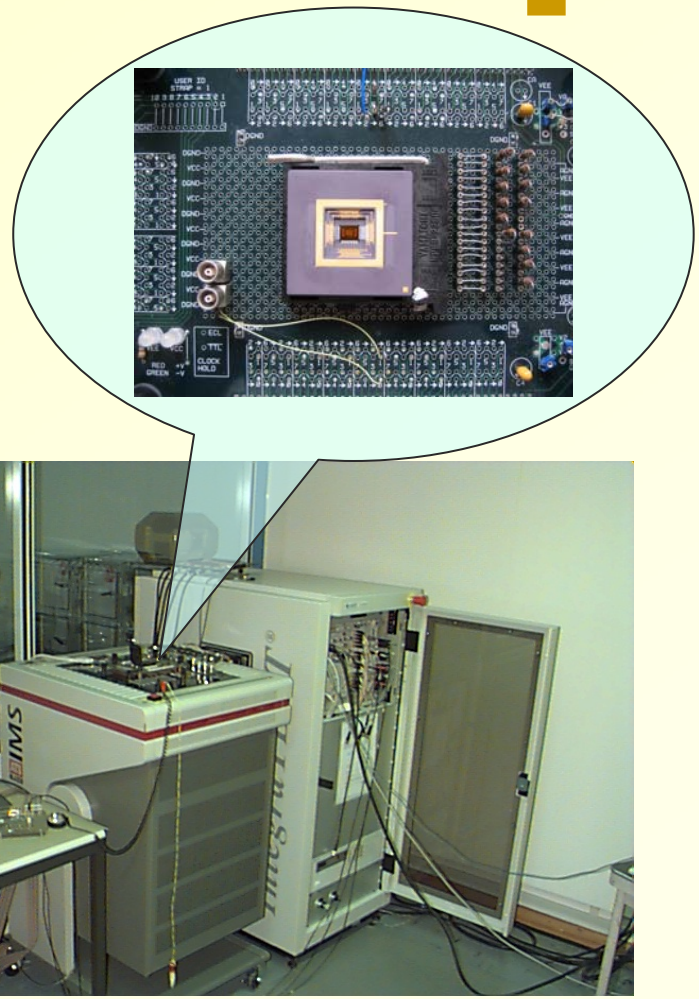
Kchip Packaging

- 196 fpBGA package
- The same package as the CCU chip
  - No cost for engineering a custom package



Prototype Tests

- Scope
  - Test functionality & validate specifications conformity.
- Method
  - Make use of a Digital Tester at CERN (MIC group).
  - Use a generic “Test Fixture” board to host the chip.
  - Use a ceramic package (CPGA) to facilitate bonding.
  - “Test Vectors” were generated from Front-End system simulations.



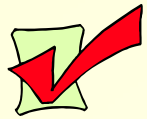
Working on the digital tester

- S. Bonacini

Kostas

Kchip V3a Prototype Test Results

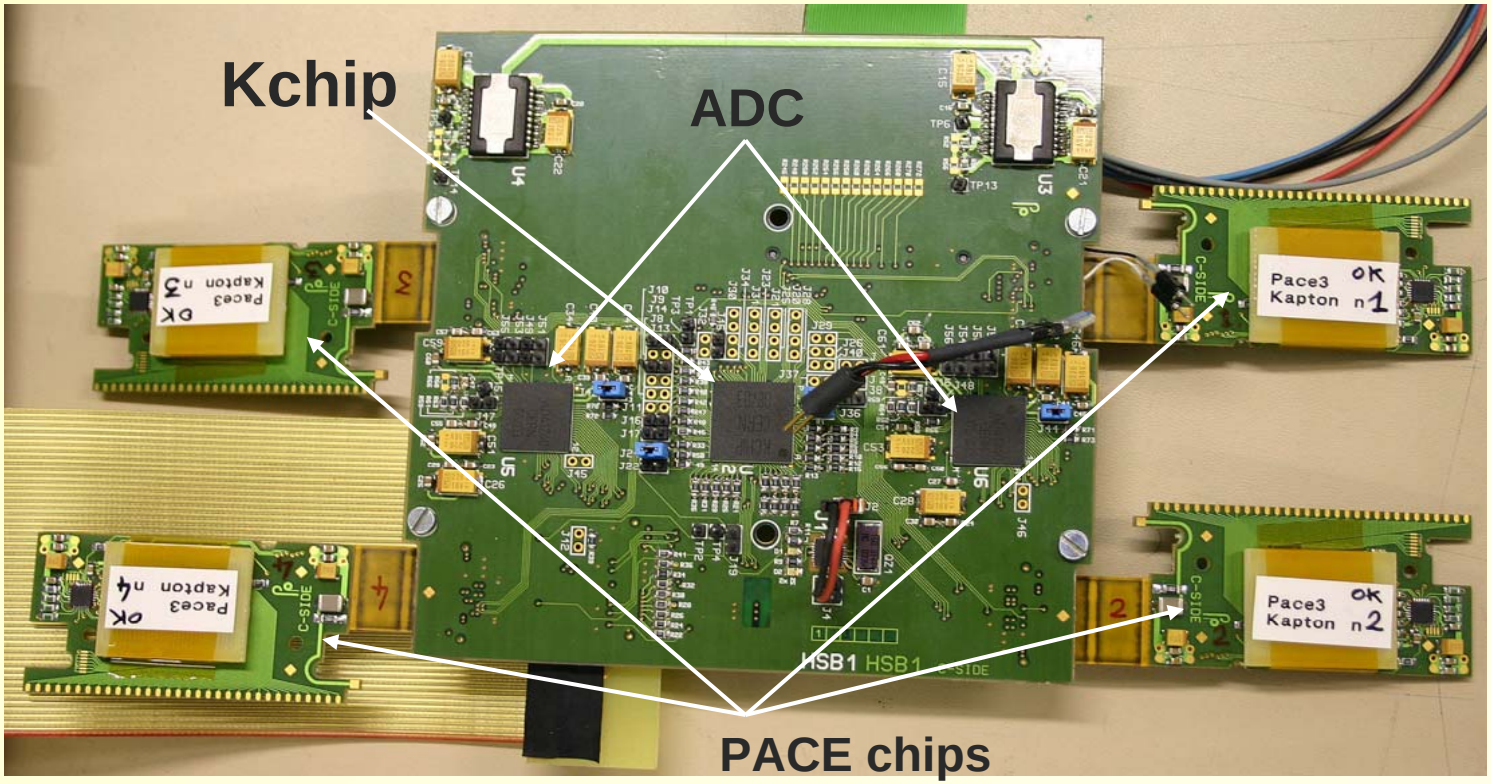
Oct. 16, 2003



- Functionality of the Kchip successfully verified with the use of a Digital Tester.
  - Various data traffic patterns were simulated and test vectors were loaded to the tester for verification.
    - All modes of operation have been verified.
    - No loss of readout synchronization up to 200KHz trigger rate (Poisson distribution).
  - I^2C Interface
    - I^2C interface maximum speed: 3.33 Mbit/s.
    - Event read/write to FIFOs.
    - Kchip has been tested with the CCU chip.
    - All Internal Registers were accessible. ID fuse bits were read out.
  - Calibration Event Generation Logic
    - Verified the Programmable Timing of the CalPulse (on chip DLL)
- Functionality of the Kchip successfully verified in system using the "half system board". (PACE - AD41240 V1 – Kchip V3a)
- Irradiation Tests
  - Use of an X-ray machine at CERN.
  - Step Irradiation at 1, 3, 5, 10, 20 MRad (SiO_2) @ Dose Rate = 2.04 MRad/h
    - Devices were operational up to 20 MRad @ 2.5V, 40MHz
- A layout bug in the Data FIFO SRAM module has been identified.
  - In specific traffic conditions, some data packets (0.5%) had errors in the data field.

Prototype System Tests

- The Half System Board
  S. Reynaud et al.



Changes in Kchip V3b

- SRAM bug
  - Layout of the macro cell is modified.
  - Stronger drivers for the SRAM (RA, WA) address buses.
- I^2C I/O pads with hysterisis.
- Configuration Registers Default values
  - CalPulse_WIDTH = 'd2
  - CalPulse_DELAY = 'b11111110
  - ADC pipeline depth ('d6)
- Hamming encoding to the SRAMs
- Built-In Self Test (BIST) to the SRAMs
- Divide the scan path to reduce production testing time.
- Impact on Design
  - Core Logic has expanded by 8%.

Kchip V3b Prototype Test Results

Mar. 16, 2004

- SRAM bug is fixed !
  - No packet output errors found
  - Patterns that produced maximum number of errors in V3a don't produce any in the present version V3b.
  - Tested with and without Hamming encoding
- Built-In Self Test (BIST) works properly
  - Identified 1 failing chip out of 10 that have been tested
    - Stuck-at-1 fault present in one of the Data FIFOs
- Hamming encoding ok
  - The chip with a stuck-at-1 doesn't give any output error because is corrected by Hamming
  - Switching off the Hamming encoding results in erroneous packet output data (for the failing chip)

Kchip V3b Prototype Test Results

- The functionality of the Kchip has been successfully verified.
  - All modes of operation have been verified.
  - No loss of readout synchronization up to 200KHz trigger rate (Poisson distribution).
  - I^2C Interface
    - I^2C interface maximum speed: 3.33 Mbit/s.
    - Event read/write to FIFOs
    - All Internal Registers were accessible.
    - ID fuse bits were read out.

Kchip V3b Prototype Test Results

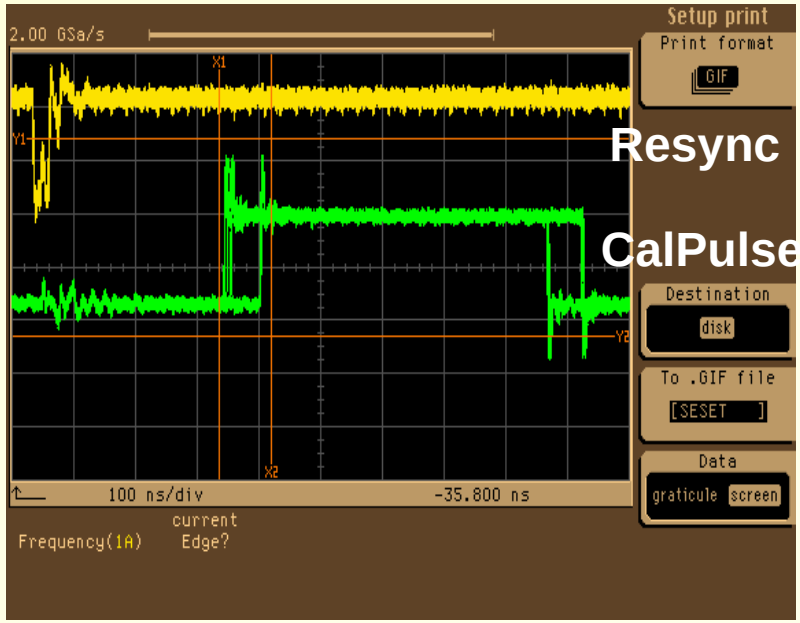
- *Difficulty in the DLL circuit of the CalPulse generation.*

- Tests performed on the digital tester.
- Using the same test vectors as for V3a.
- The DLL is not able to maintain lock.
- The DLL locks when operating the chip at 25MHz at 2.5Volt.

- The problem has been identified and accounted to be an artifact of the test vector sequencing on the tester.
  - There is a pause of 40 clock cycles when the test vector sequence rolls over to the beginning of the pattern.
  - Tests were completed successfully when we provided a continuous clock.

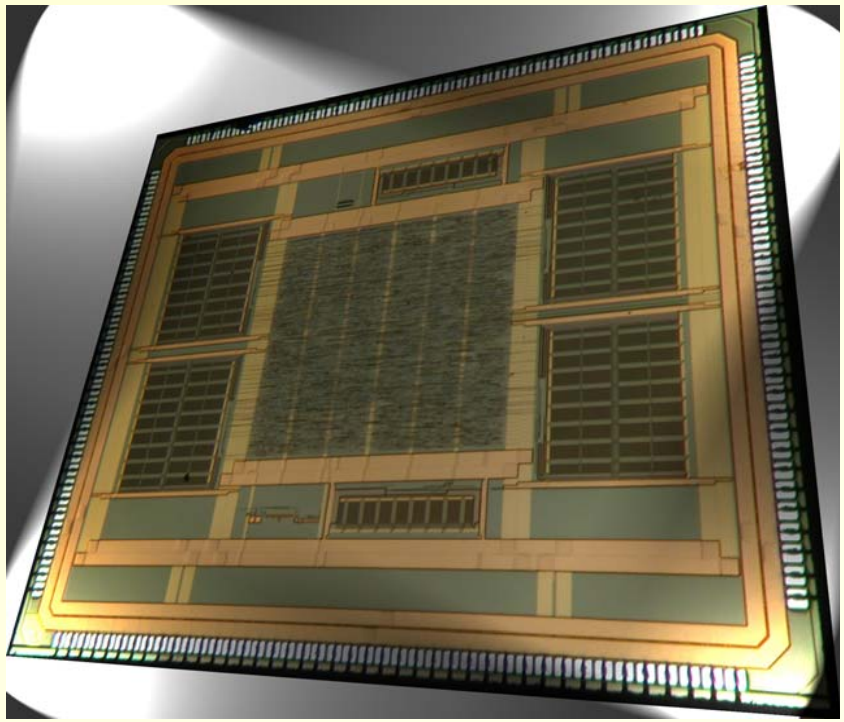
- The same DLL circuit was used in version V3a and was able to maintain lock despite the missing clock cycles.

- Might be a process specific problem.



Kchip V3b Prototype Test Results

- Power consumption
  - Test Conditions: 40MHz, VDD=2.5V, T=25^{O}C, 100kHz-trigger.
  - I_{core} = 78mA, P_{core} = 195mW
  - I_{peri} = 195mA, P_{peri} = 487mW
  - I_{total} = 273mA, P_{total} = 682mW
  - Overall 9% increase in respect to Kchip V3a



Planning

- Package Kchip V3b chips in fpBGA packages should be shipped by ASAT on the 10th of May.
- In-system tests of the Kchip V3b on the “Preshower motherboard”
  - Verify that the Kchip interfaces correctly with the PACE_AM, AD41240 V2 and the control chips (QPLL, TPLL, CCU).
    - Known problem:
      PACE3-Kchip V3a (& V3b) column address interface mismatch.
      (PACE3 transmits column addresses in GRAY code!)
    - Problem has been bypassed by swapping the LVDS column address lines, effectively inverting the logic state of the line.
  - Evaluate the Kchip V3b functionality in the system.
  - Very important step before submitting the Kchip for an engineering run.
- Perform Total Dose Irradiation tests on Kchip V3b.

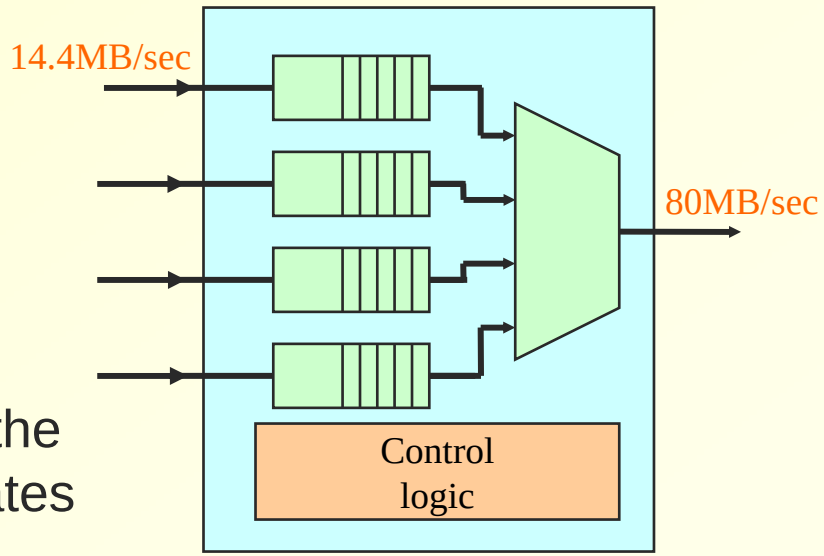
Backup Slides

Data Rates

- PACE generated traffic

3 columns/trigger
32 samples/column
} 96 samples/trigger
12-bit ADC
100KHz Trigger Rate
} 14.4 MB/sec

Traffic from 4 PACE chips = 57.6MB/sec



- Gigabit Link Throughput

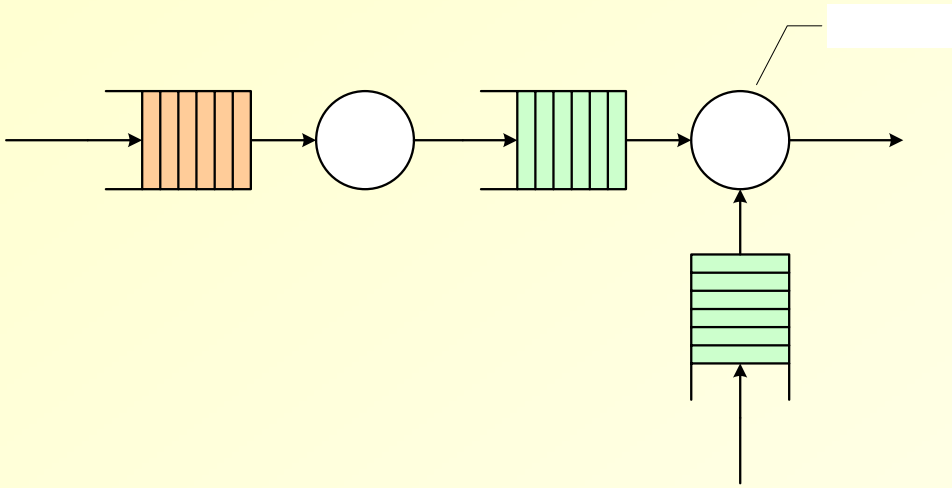
(GOL chip) 80 MB/sec

PACE event readout time = 6.9 μsec
Kchip event readout time = 7.8 μsec

- The difference in the readout times and the stochastic nature of trigger arrivals mandates the need of data buffering on the Kchip.

Front-End System FIFOs

- Model of front-end system FIFOs.



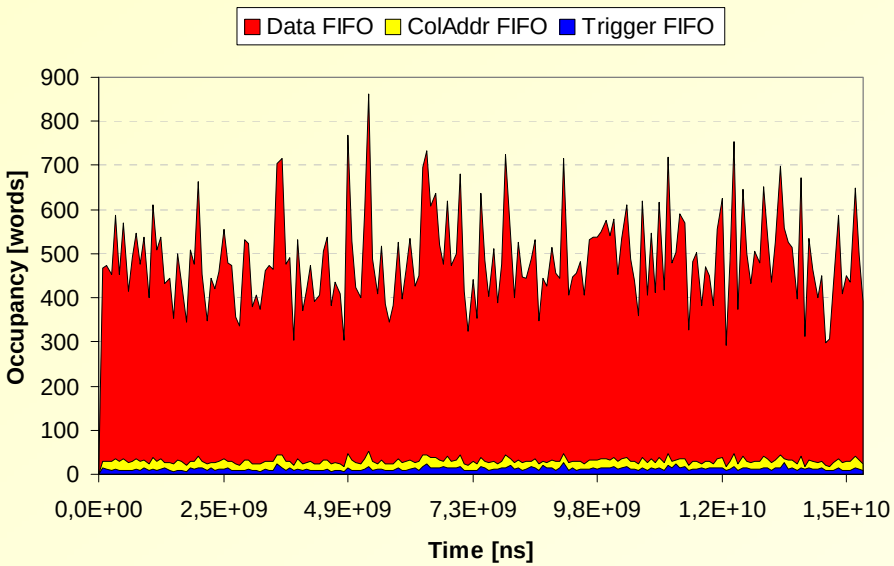
- Trigger arrivals follow an exponential distribution.
- Kchip service time follow a uniform distribution. PACE FIFO
  - An analytic queuing model is difficult to develop.
  - A simulation model of the complete front-end system has been developed.

λ_{LV1}

μ_P

Sizing the Kchip FIFOs

- PACE FIFO can store up to 10 events.
  - From simulations: $P_{rejection}$= 1.9E-04 @ 100KHz trigger rate.
- Kchip FIFOs:
  - Kchip FIFOs should be sized for lower event rejection probability.

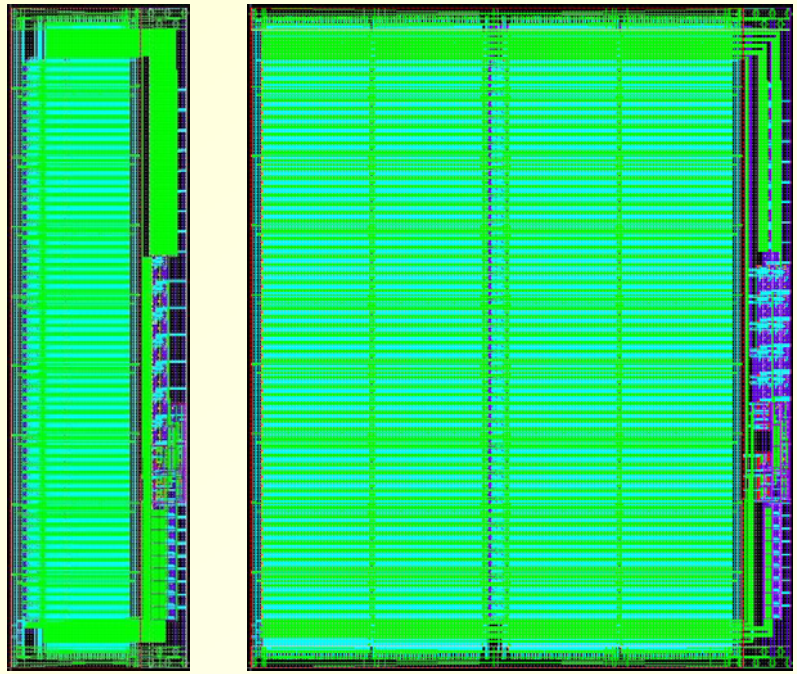


Time examined	15.10^2	s
Number of events	$1.5\ 10^6$	
Mean interarrival time of events	10.059	μs
PACE rejected events	7	
Kchip rejected events	0	
Maximum Trigger FIFO occupancy	26	words
Maximum Column FIFO occupancy	52	words
Maximum Data FIFO occupancy	863	words
Average Trigger FIFO occupancy	3	words
Average Column FIFO occupancy	2	words
Average Data FIFO occupancy	36	words

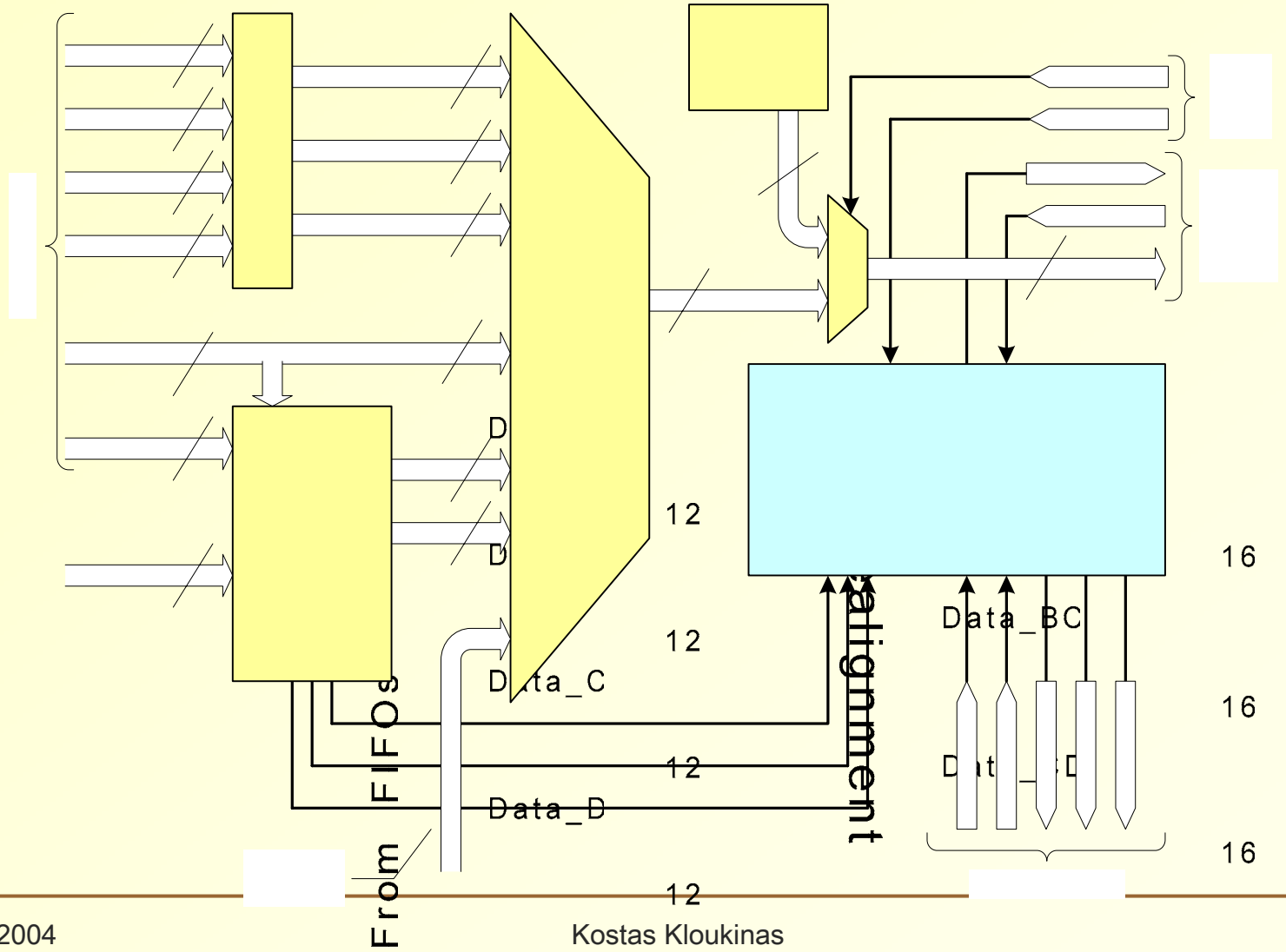
Implementation of Kchip FIFOs

FIFO	Native Size of SRAM module	Actual Capacity
Data	1 Kword x 18 bits	10 events (1024/96)
Column Address	128 words x 27 bits	10 events (matches Data FIFO)
Trigger	128 words x 27 bits	64 triggers (128/2)

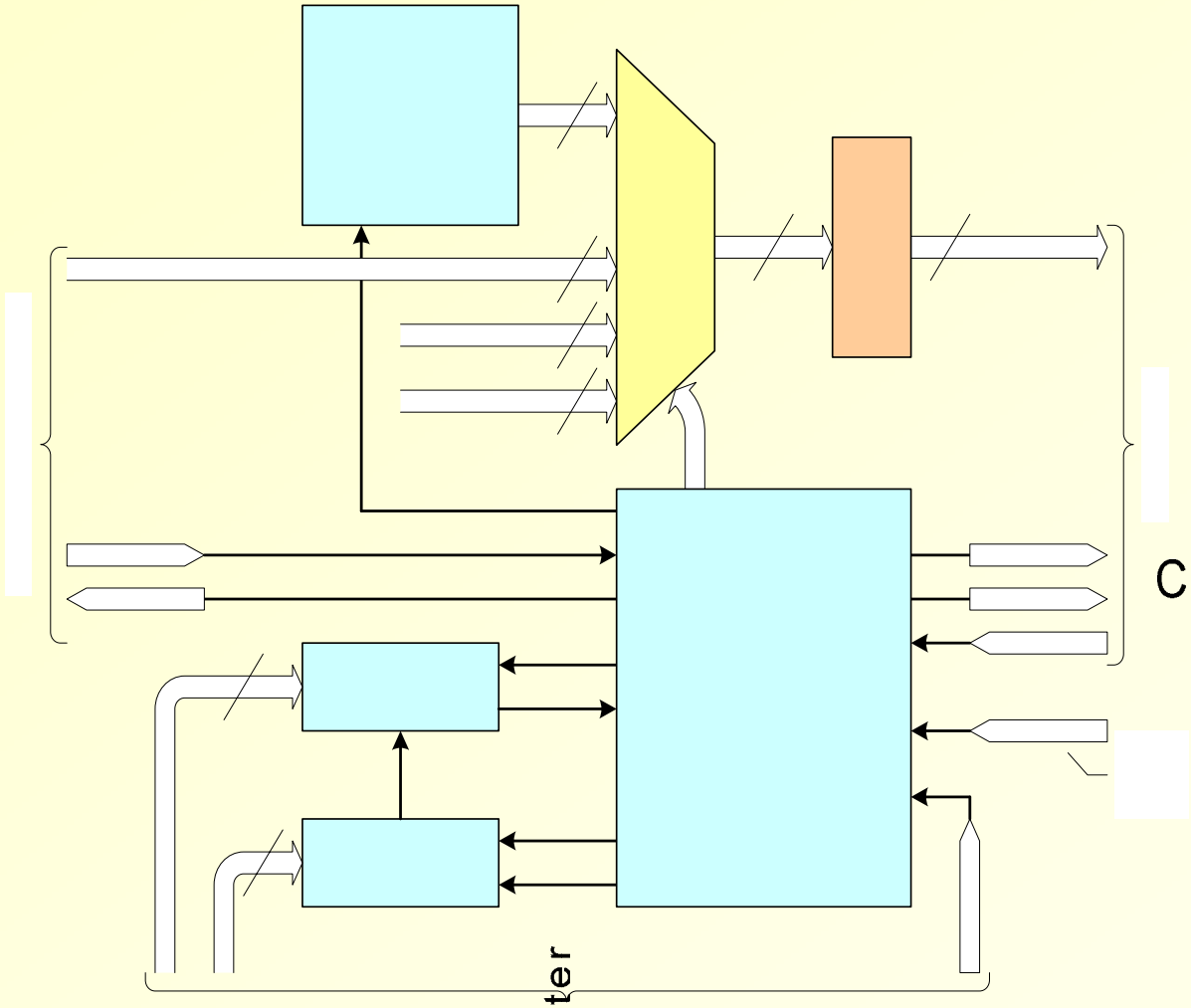
- FIFOs are implemented using a "Configurable Dual-Ported SRAM macro cell".
- Two macro cells:
  - Column Addr. & Trigger FIFO
    - 128 words x 27 bits
  - Data FIFO
    - 1024 words x 18 bits



Packet Formatter



GOL Interface



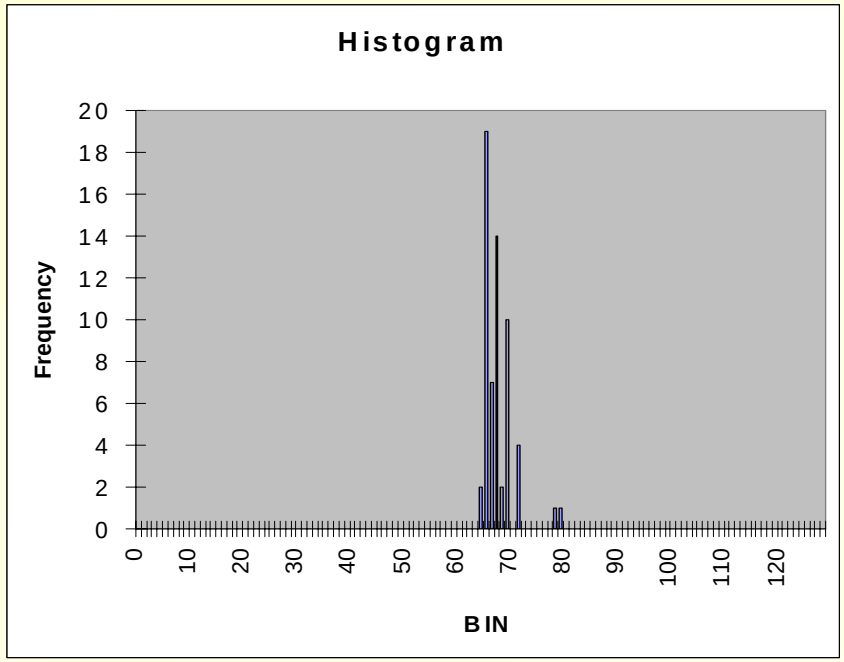
"SOF" charac

"EXT" charac

Errors in Data Packets

- Generated special test vectors to produce the following traffic:
  - Send a number of triggers spaced at 6.9μs (PACE readout time) to establish a difference between WA and RA pointers.
  - Send hundreds of triggers spaced at 7.475 μs (Kchip service time) to maintain the pointers difference through out the test.

- Error generation is more pronounced when the difference between the WA and RA pointers is ~64 locations !
  - Indication that the error comes from the address decoding of the 6th address bit



Test Pattern sequences

- (a) Kchip in Test Mode
  - Access on-chip FIFOs and internal registers through the I^2C interface.
- (b) Kchip in Test Mode
  - Filling the on-chip FIFOs from the ADC bus and then reading data back through the I^2C interface.
- (c) Kchip in Test Mode
  - Loading data into the FIFOs through the I^2C interface and then reading it out from the GOL bus.
- (d) Kchip in Normal Mode
  - Sending triggers and reading out events through the GOL.