2nd Kchip Design Review

CERN

Jan. 17, 2003

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EP/CME-PS

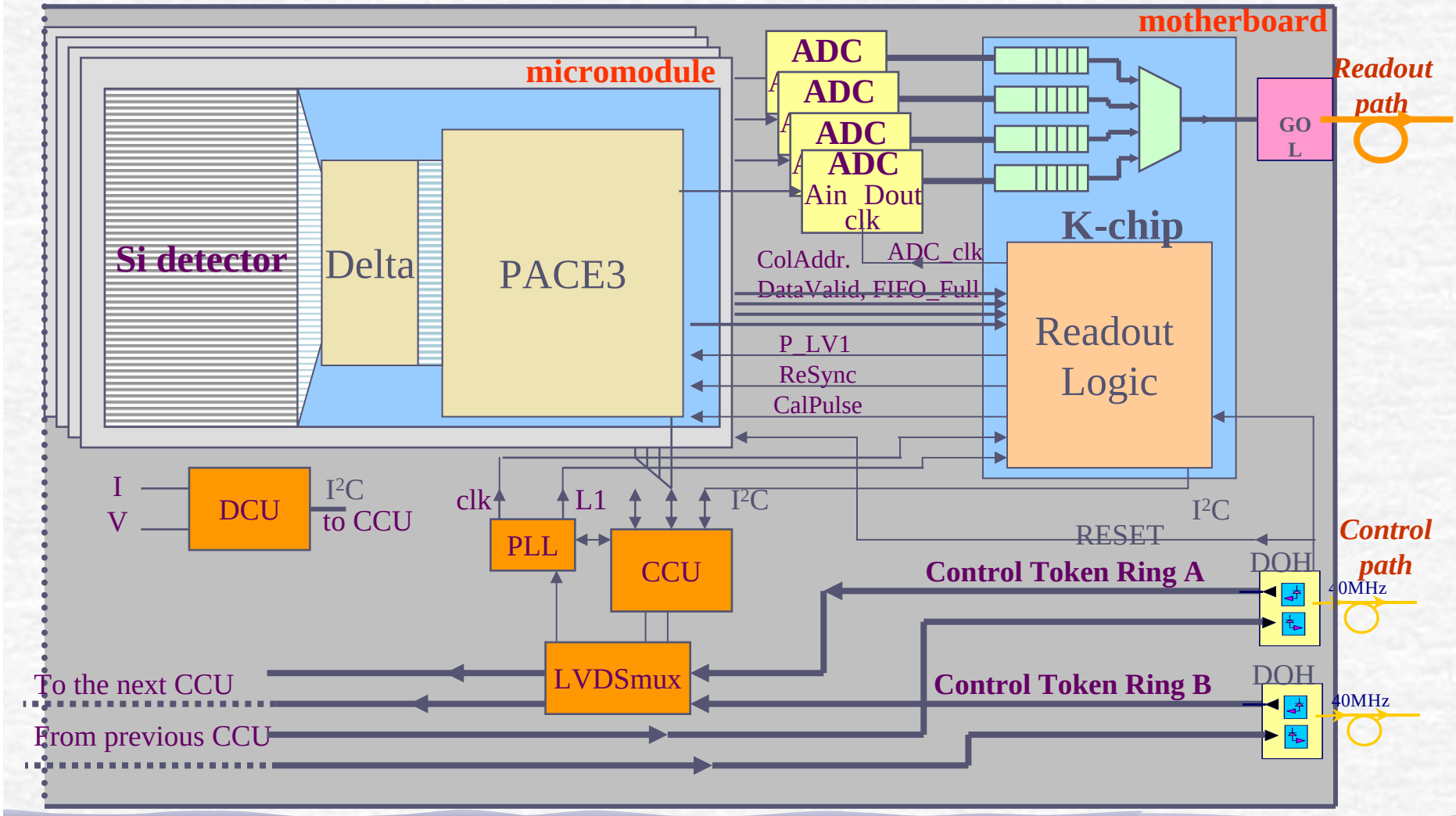
Introduction

- 1st Kchip Design Review
  - Oct. 11, 2002
  - Issues reviewed:
    - Architecture
      - Interfaces with PACE, ADC, GOL, I^2C.
      - SEU protection techniques.
    - Functionality
      - Data Flow.
      - Buffer Overflow Handling.
      - Packet Format, Error Handling.
- Kchip Design Team
  - Kostas Kloukinas, EP/CME-PS
  - Sandro Bonacini, EP/MIC-DG

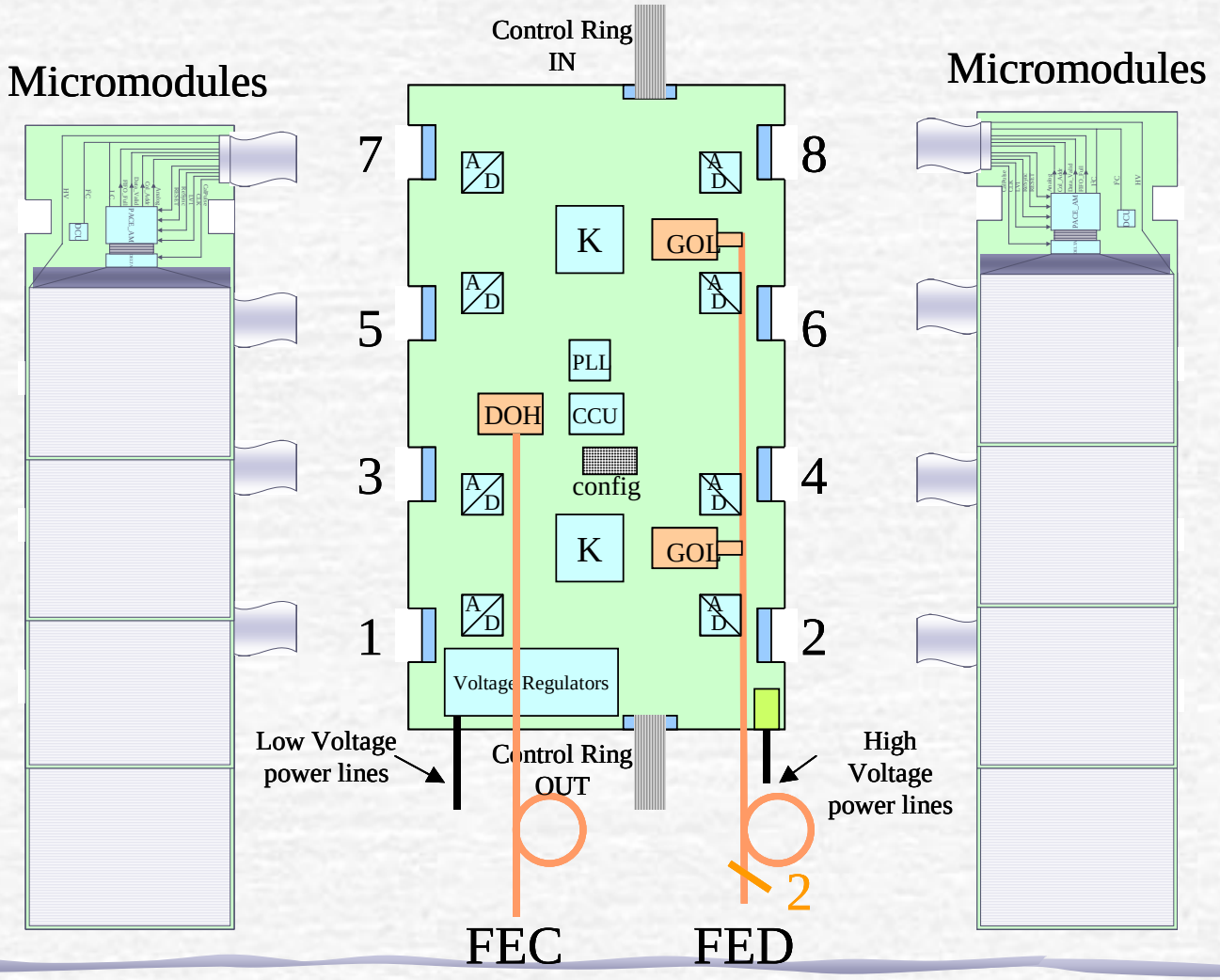
Outline

- Architecture of the chip
- Functionality of each block
- Silicon Implementation
- Design status & planning

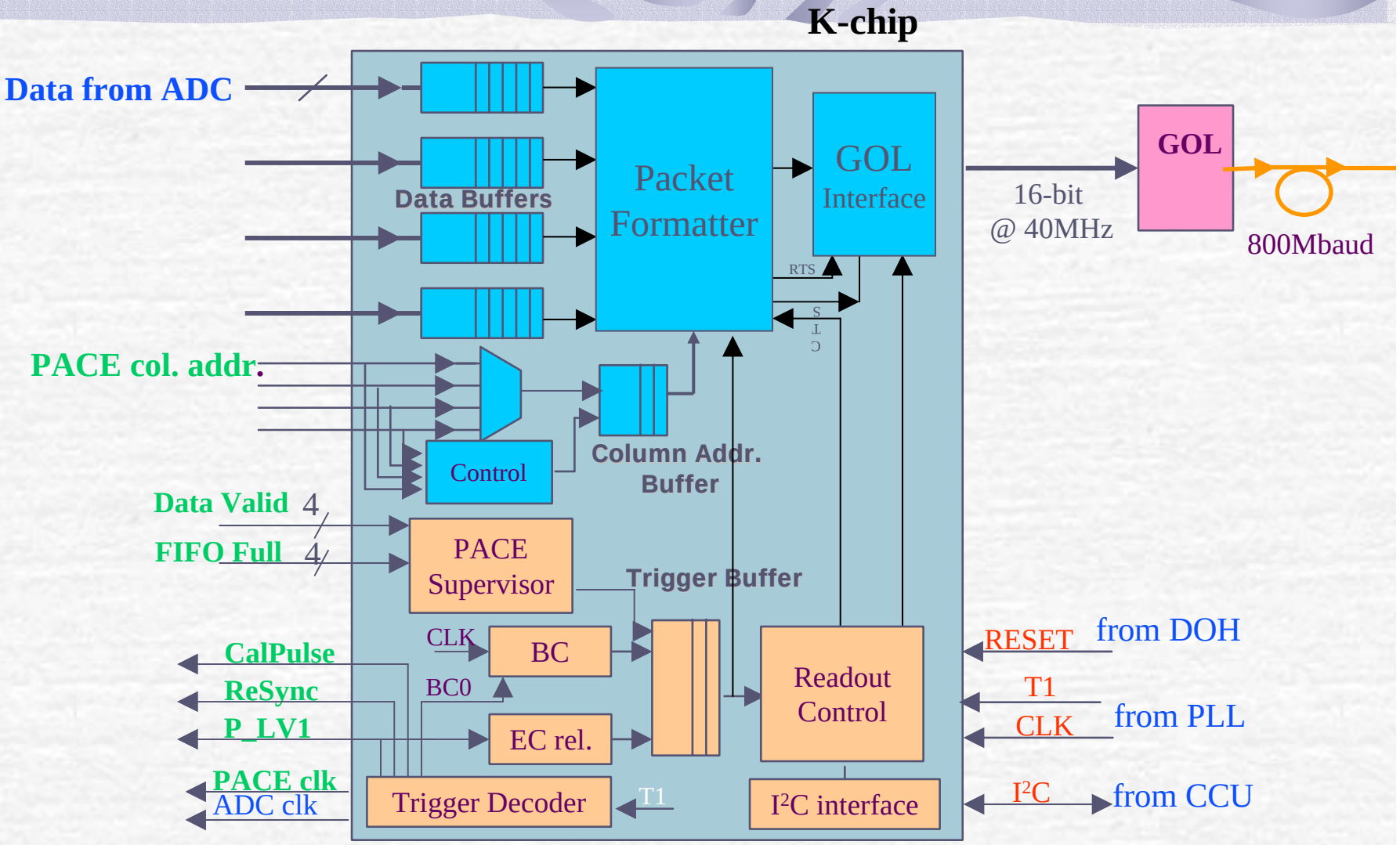
The Preshower FE System



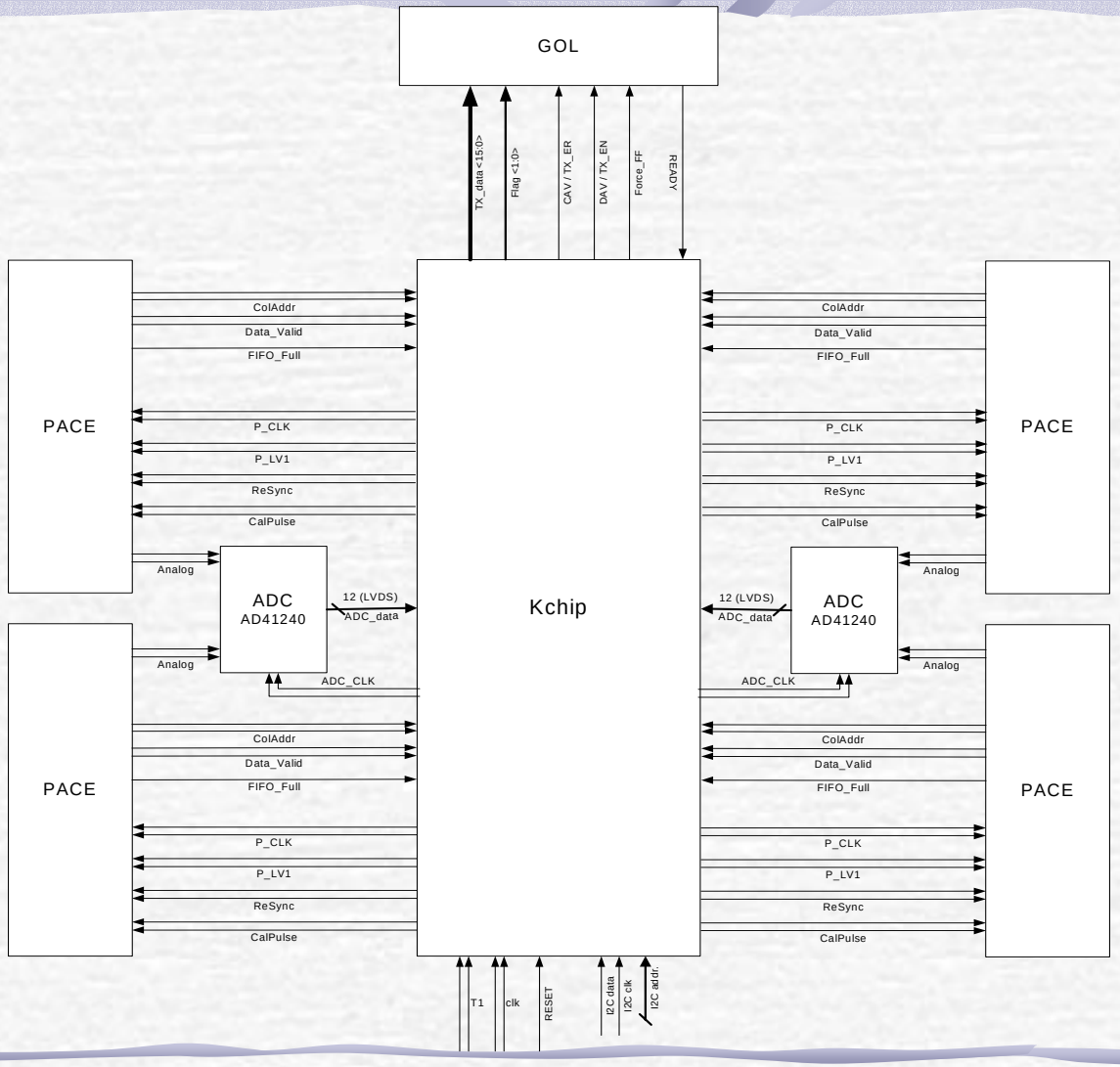
The Preshower FE System



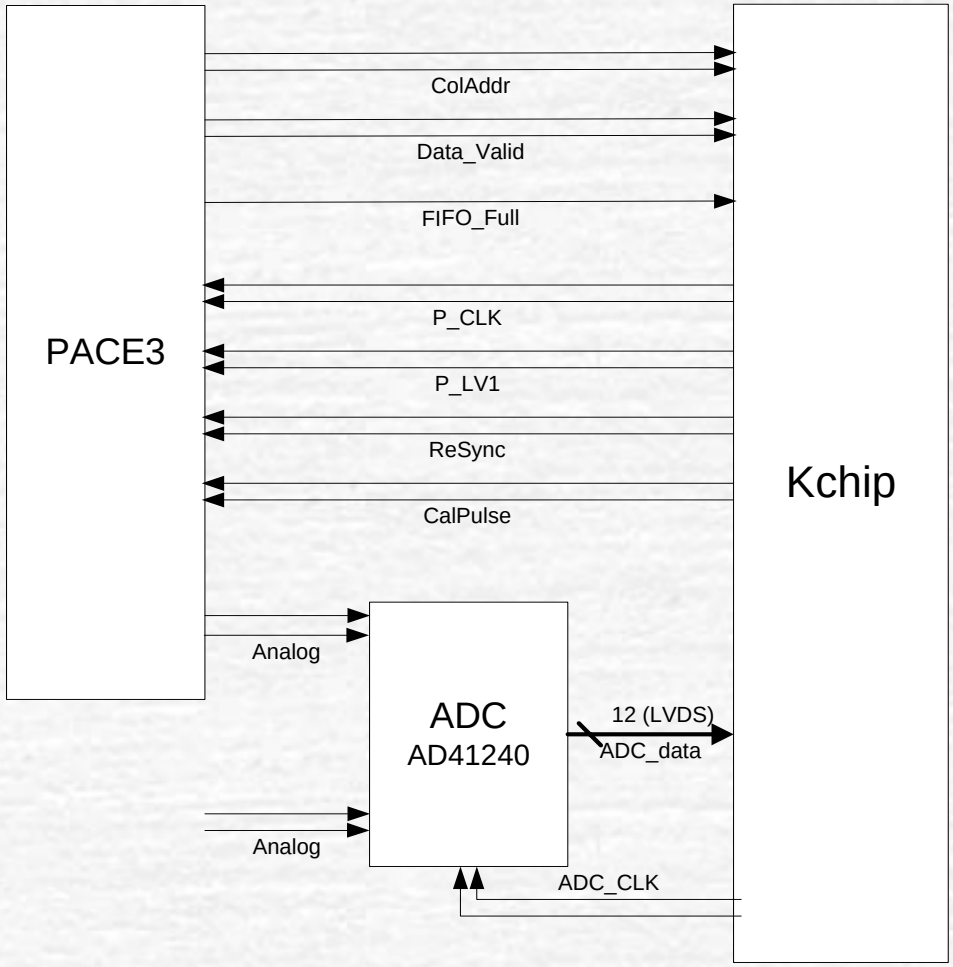
Kchip Block Diagram



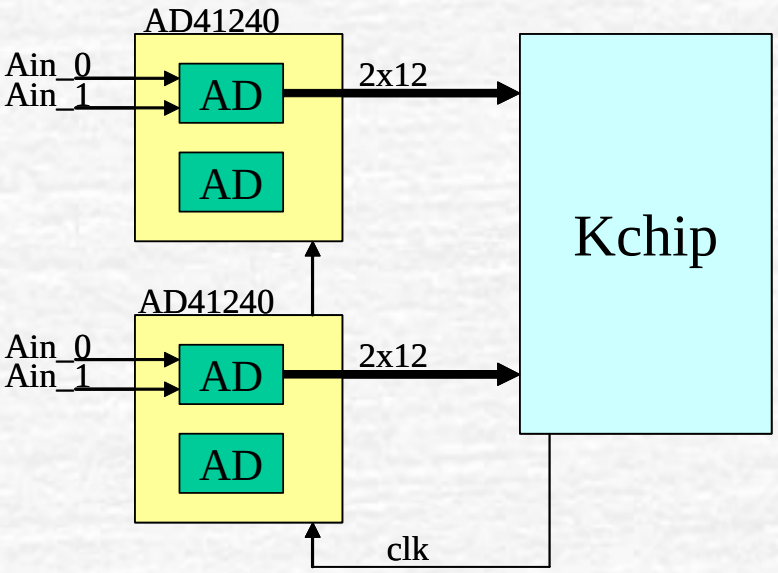
Kchip Interfaces



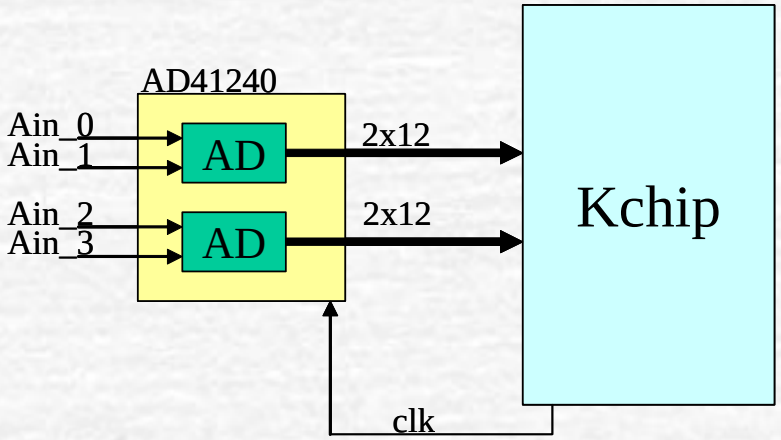
PACE & ADC Interface



ADC interface options

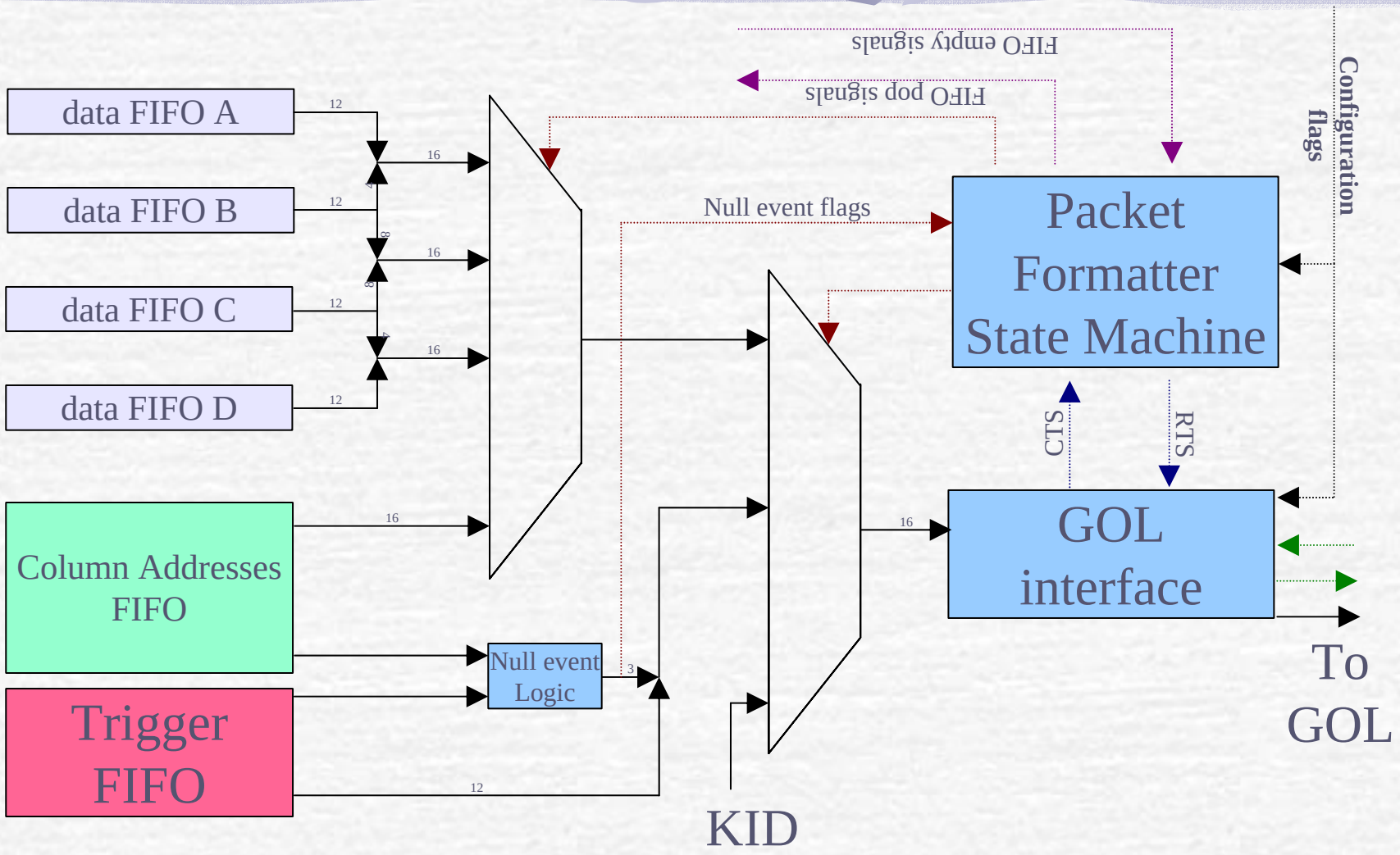


a) 2 x dual channel ADC

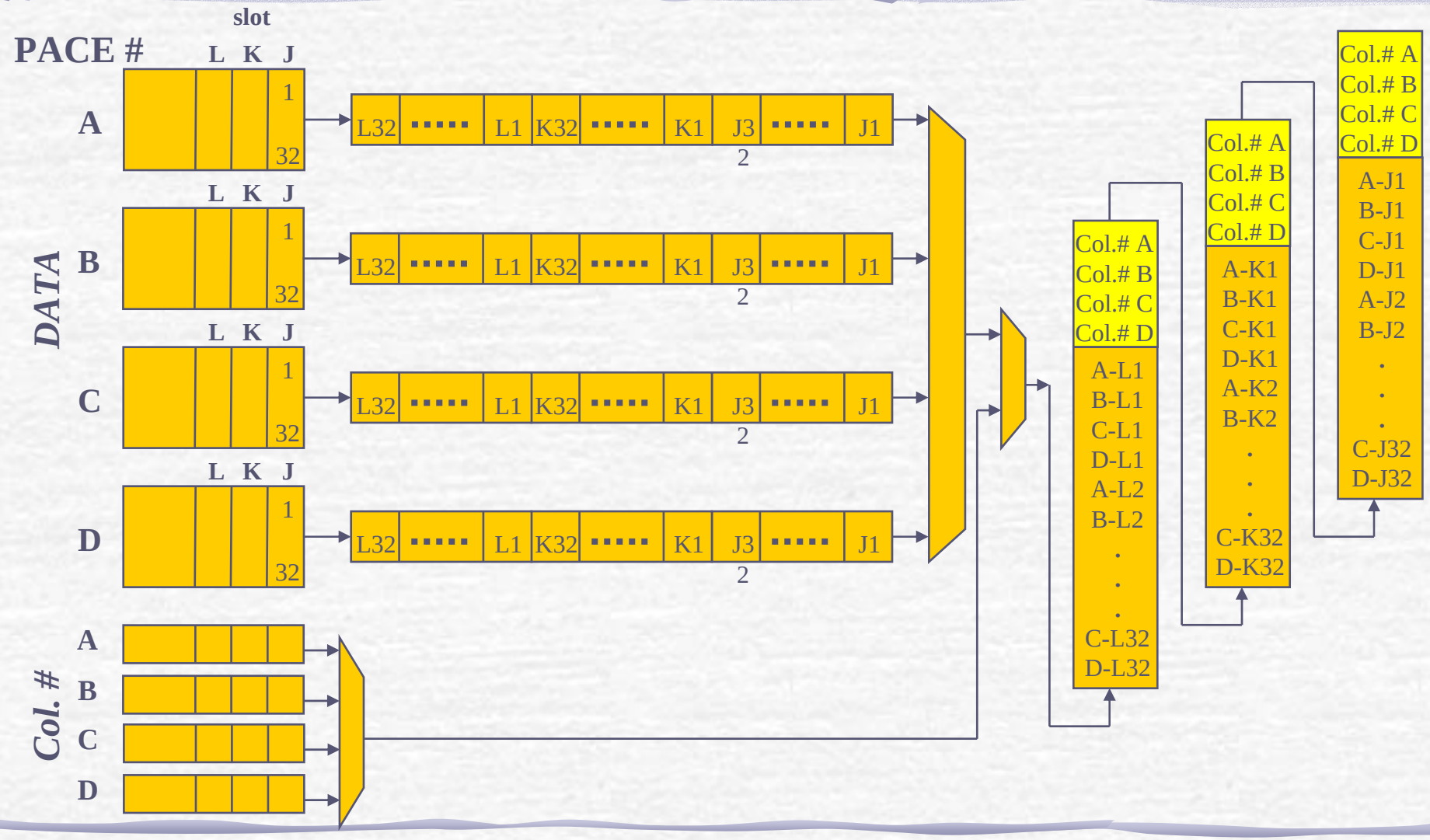


a) 1 x quad channel ADC

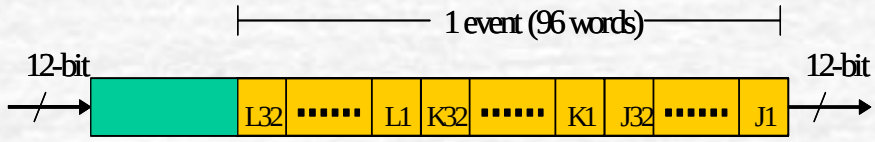
Data Path


FIFO empty signals
FIFO pop signals
Configuration flags
data FIFO A
data FIFO B
data FIFO C
data FIFO D
12
16
Null event flags
Packet Formatter State Machine
CTS
RTS
Column Addresses FIFO
Null event Logic
3
GOL interface
To GOL
Trigger FIFO
KID

Data Formatting

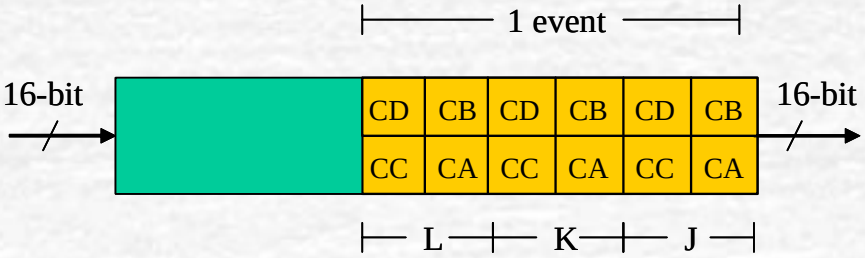


Kchip FIFOs



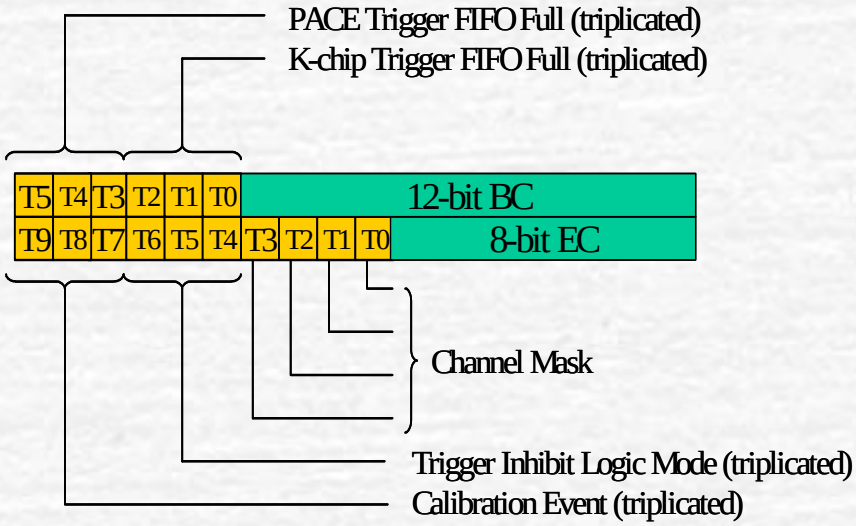
Memory Slots per event : J,K,L
Samples per slot : 1..32

Data FIFO
96 words/event



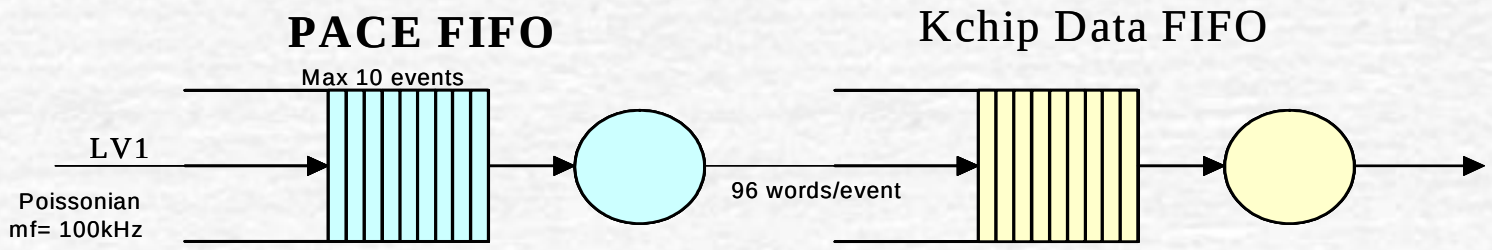
Memory Slots per event : J,K,L
Samples per slot : 1..32

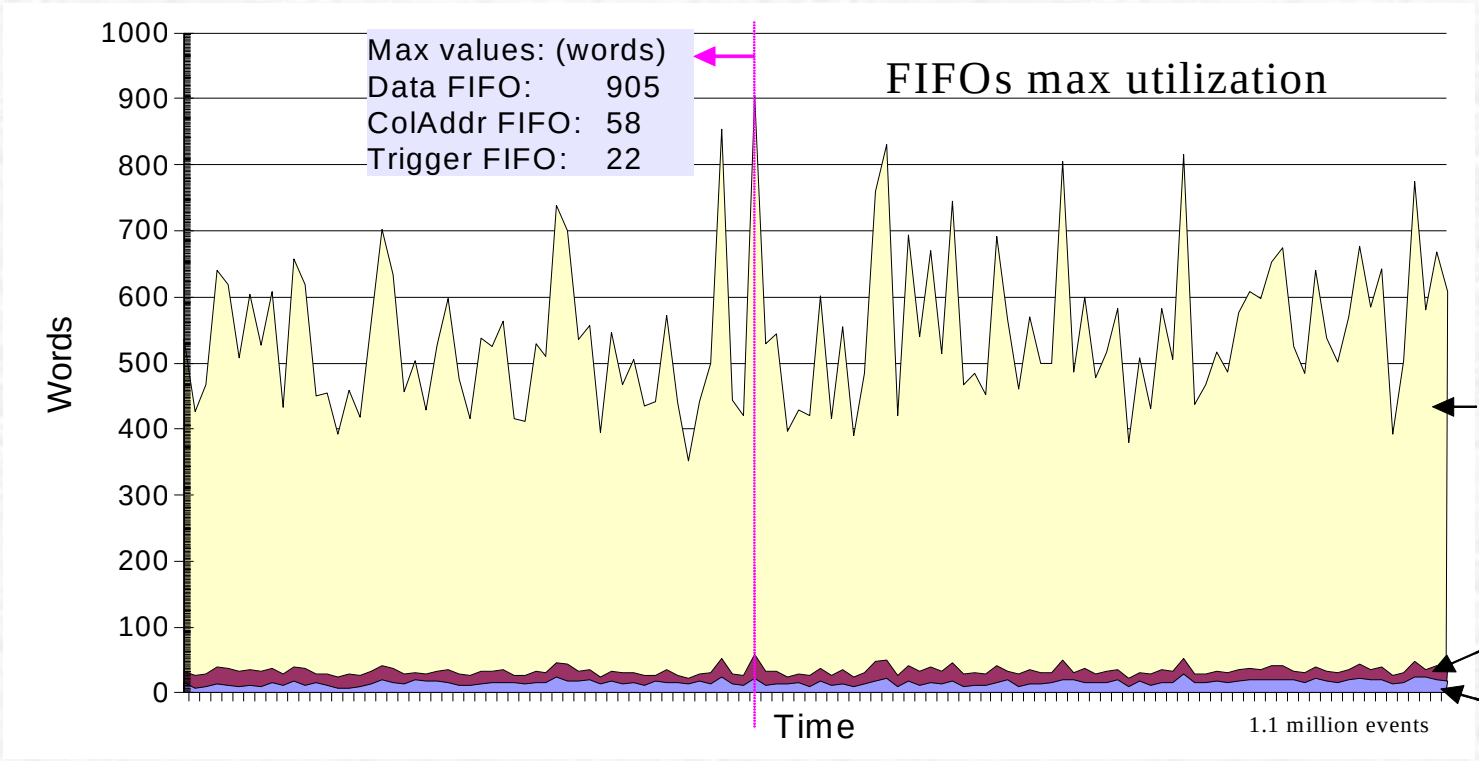
Column Address FIFO
6 words/event



Trigger FIFO
2 words/trigger

Sizing the Kchip FIFOs

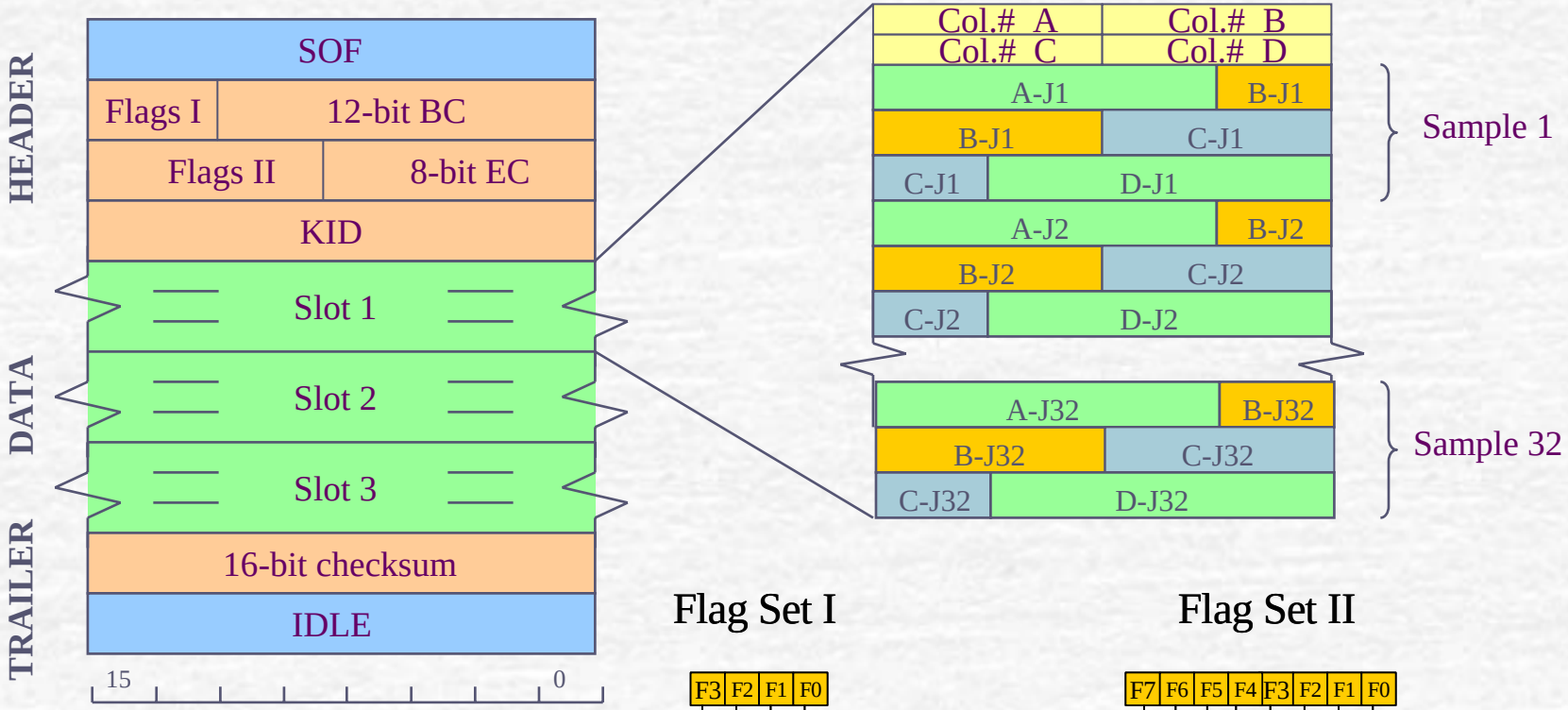




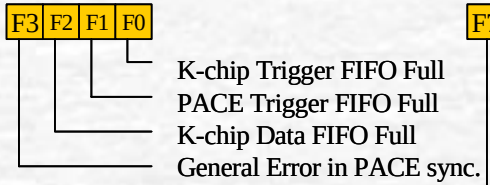
Kchip FIFOs

FIFO	Native Size	Actual Capacity
Data	1 Kword x 18 bits	10 events (1024/96)
Col. Addr.	128 words x 27 bits	10 events (matches Data FIFO)
Trigger	128 words x 27 bits	64 triggers (128/2)

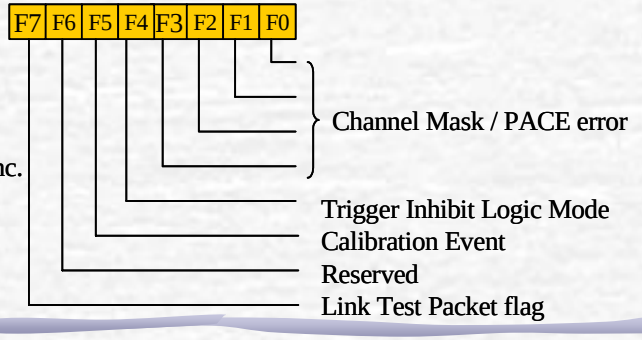
Packet Format



Flag Set I

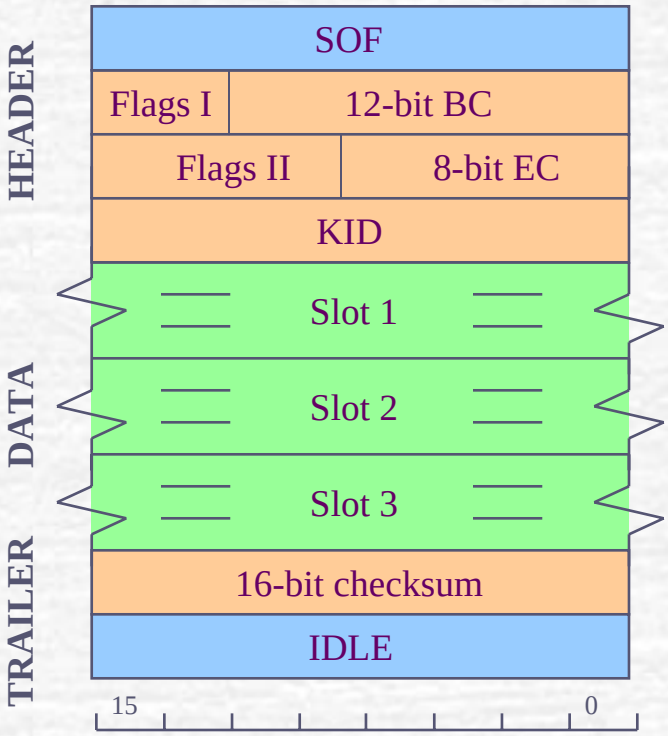


Flag Set II

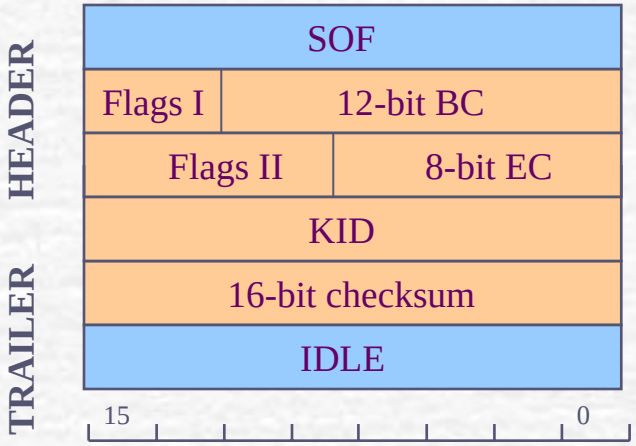


Packet Types

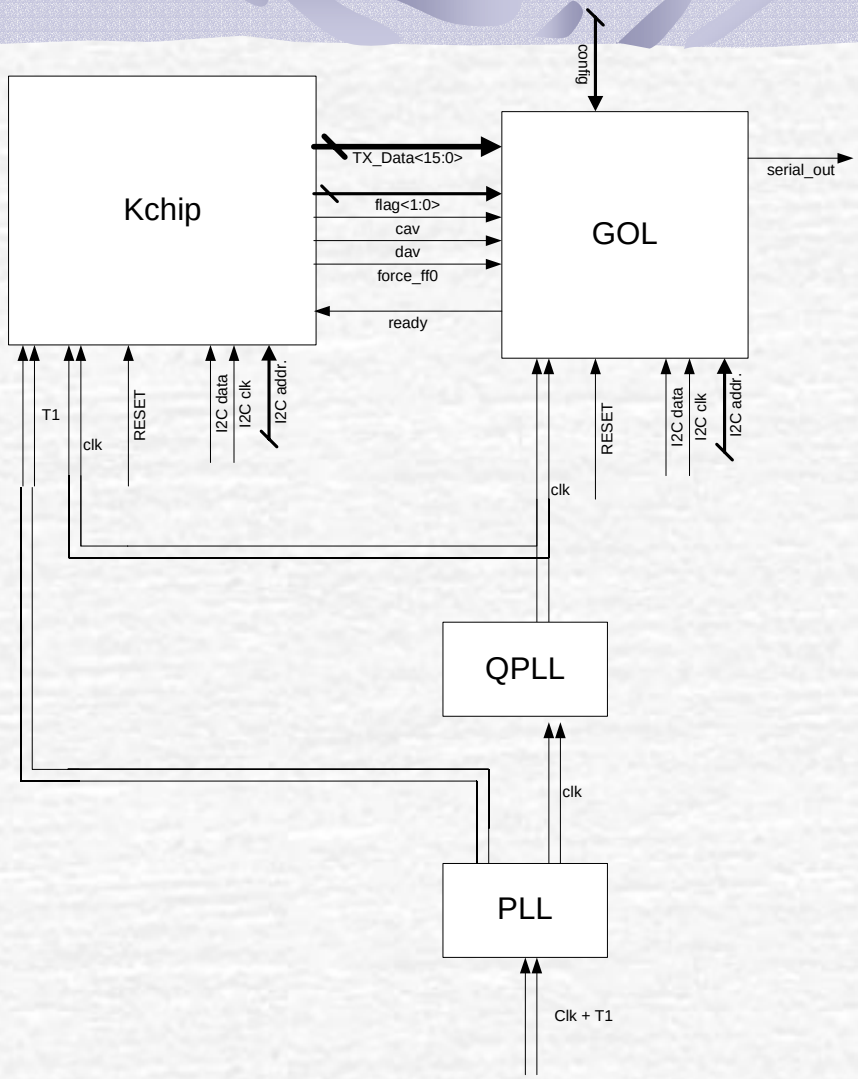
Normal Event



Null Event



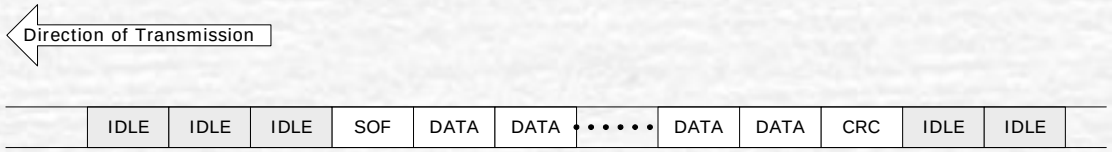
Kchip GOL Interface



Link Layer

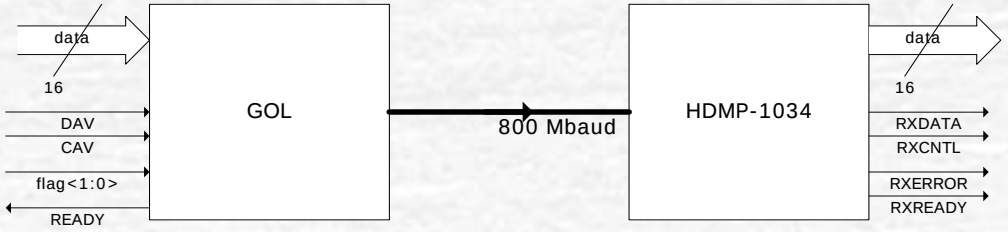
- The Kchip employs a character oriented data transmission protocol. To achieve character synchronization the Kchip uses two uniquely defined transmission control characters, the IDLE and the SOH.
- The IDLE character has two functions.
  - Firstly, allows the receiver to obtain and maintain bit synchronization.
  - Secondly, allows the receiver to obtaining character synchronization.
- The SOF character indicates the beginning of the frame and delimits the boundaries of subsequently transmitted frames (back-to-back transmission).

General Frame Format

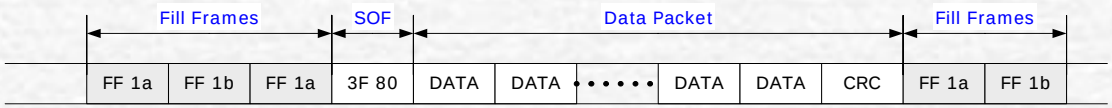


- The Kchip supports two encoding schemes: the CIMT and the 8b/10b encoding.
  - The flexibility of using both encoding schemes is realized by properly choosing the transmission control symbols (SOF, IDLE) which are supported in both encoding schemes.
- Use of CRC-CCITT polynomial: $x^{16} + x^{12} + x^5 + 1$

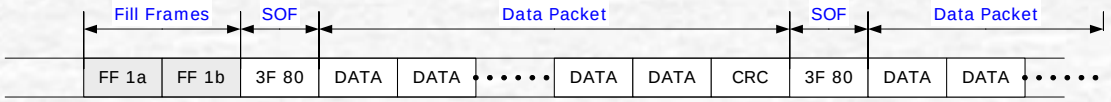
Using CIMT protocol



Link structure (serializer-deserializer) when using CIMT protocol.

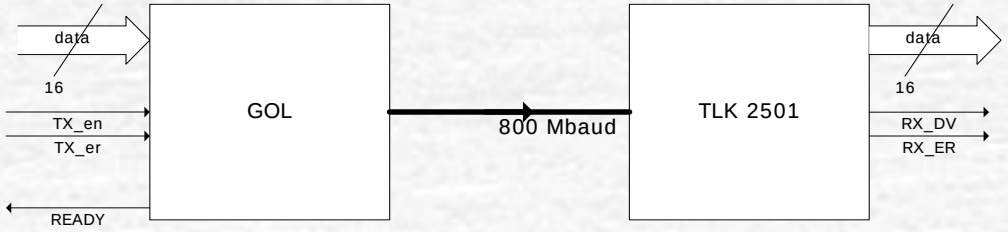


Packet format in CIMT protocol.

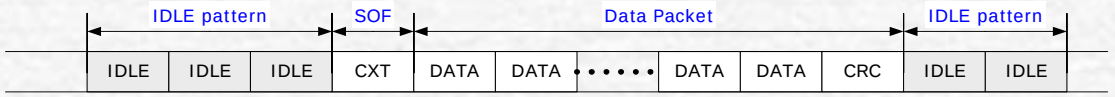


Packet format in CIMT protocol for back-to-back events.

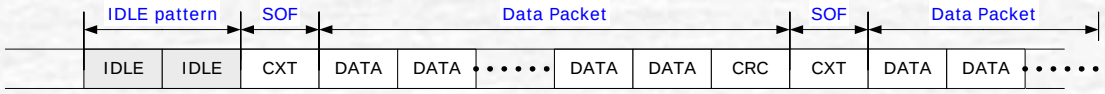
Using 8b/10b encoding



Link structure (serializer-deserializer) when using 8b/10b encoding protocol.



Packet format in 8b/10b protocol.



IDLE = <K28.5, D5.6> or <K28.5, D16.2> : Idle
CXT = <K23.7, K23.7> : Carrier Extend

Packet format in 8b/10b protocol for back-to-back events.

Link Synchronization

- The Link can be synchronized by transmitting a stream of IDLE character.
- To help maintain synchronization the Kchip:
  - transmits IDLEs when no data are available.
  - can insert a programmable number of IDLEs in the data stream in programmable intervals.
- The Kchip features a “Link Test” mode where:
  - Data traffic can be generated continuously using a specific “Link Test packet” or
  - A user defined event can be upload through the I2C bus and then transmitted through the link.

Trigger Decoder

- The Kchip has a trigger decoder logic that decodes the trigger commands.

Pattern	Command
100	LV1A (Trigger Level 1 Accept)
110	CalPulse (Calibration)
101	ReSync (Reset FE Pipelines)
111	BC0 (Bunch Crossing Zero identifier)

For debugging purposes there are:
• Trigger Mask register that can mask individually specific trigger commands.
• Last Trigger Command register to check the last issued command.

- The actions taken by the Kchip logic when a Trigger Command is issued are listed:
  - **LV1A:** sends an trigger pulse to the PACE3 chip and increments the EC and inserts a normal event in the trigger FIFO.
  - **CalPulse:** send a calibration pulse to the PACE3 chip and starts countdown of the latency counter. Upon timeout it increments the EC and inserts a calibration event in the Trigger FIFO.
  - **ReSync:** resets the EC and BC and clears the Data, Column and Trigger FIFOs. Resets PACE supervisor logic error flags.
  - **BC0:** resets the EC and BC counters.

Exception Handling

- Buffer Overflow
  - FIFOs can overflow both in the PACE and in the Kchip.
- PACE out of Sync
  - Under normal operation all PACEs should run synchronously.
  - If a PACE runs out of sync. the condition is identified and signaled.

The Trigger Inhibit Logic

- Scope: to filter out triggers that will cause the PACE Trigger FIFO to overflow.
- The Kchip incorporates a PACE Trigger FIFO emulator.
- The Trigger Inhibit logic can be enabled or disabled by the user.

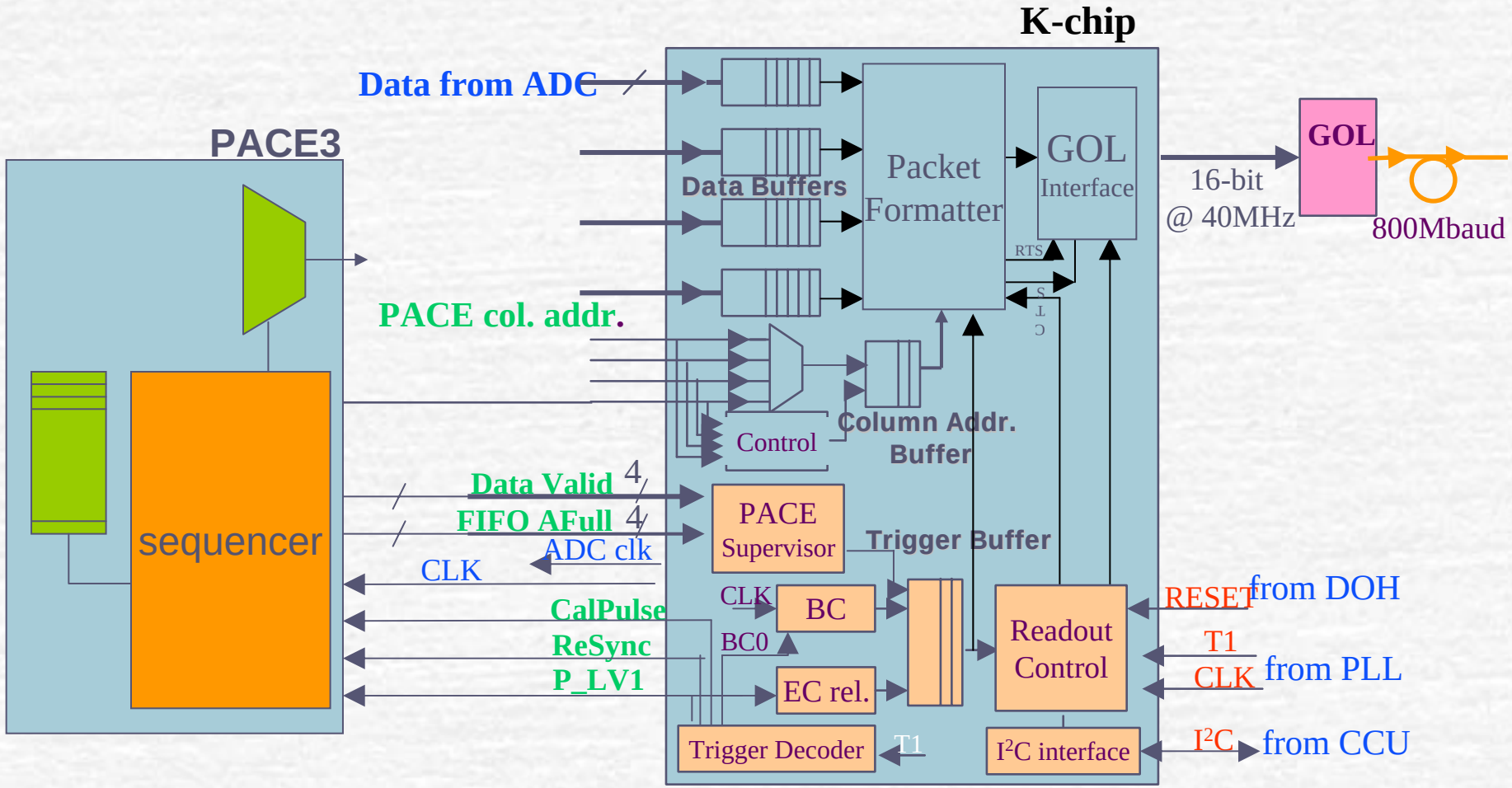
FIFO Overflow Handling

- Overflow Handling
  - If PACEs overflow then NULL events are being transmitted until the condition terminates. EC & BC tags can be used to check and maintain event readout synchronization.
  - If Data FIFO overflows then NULL events are being transmitted until the condition terminates. EC & BC tags can be used to check and maintain event readout synchronization.
  - If Trigger FIFO overflows (highly unlikely) then data transmission will be suspended until space is available to store more incoming triggers. The number of lost triggers can be estimated using the EC & BC tags on the packets before and after the overflow condition.

Exception Handling

- The Kchip supervises the syncronicity of the readout operation for the connected PACE chips by monitoring the “DataValid” and “AFIFO_full” signals.
- “PACE out of sync” condition is signaled when the readout sequence in any of PACE chips is not synchronous to the Kchip internal readout sequencer.
- The “PACE out of sync” condition is flagged in the data packet header and in a special status register accessible through the I^2C bus.

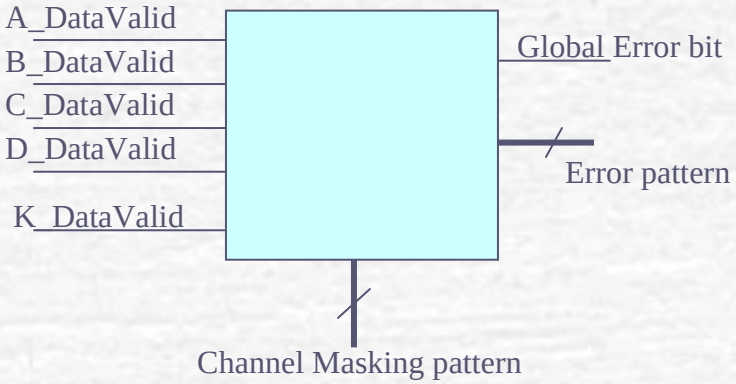
PACE3 – Kchip interface



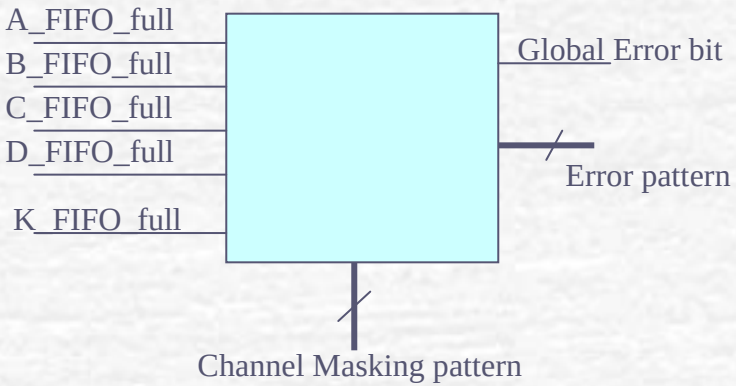
PACE supervisor in Kchip

- PACE supervisor block in the Kchip emulates the operation of the actual PACE3 sequencer.
  - Initiates a readout sequence for every event.
  - Keeps track of the number of events in the PACE3 Trigger FIFO (counting event samples).
  - Cross-checks the 4 DataValid signals.
    - Sets an error flag in that data stream upon a mismatch.
  - Cross-checks the 4 AlmostFull signals.
    - Sets an error flag in that data stream upon a mismatch.

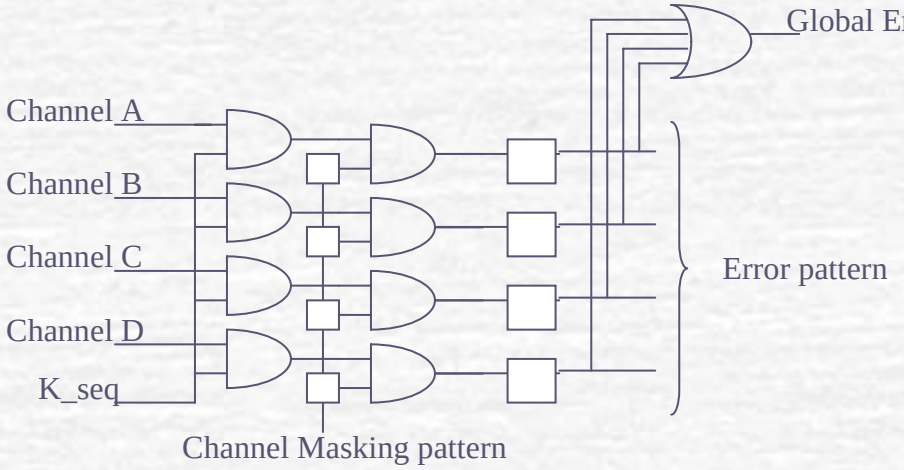
PACE Supervisor Logic



a)

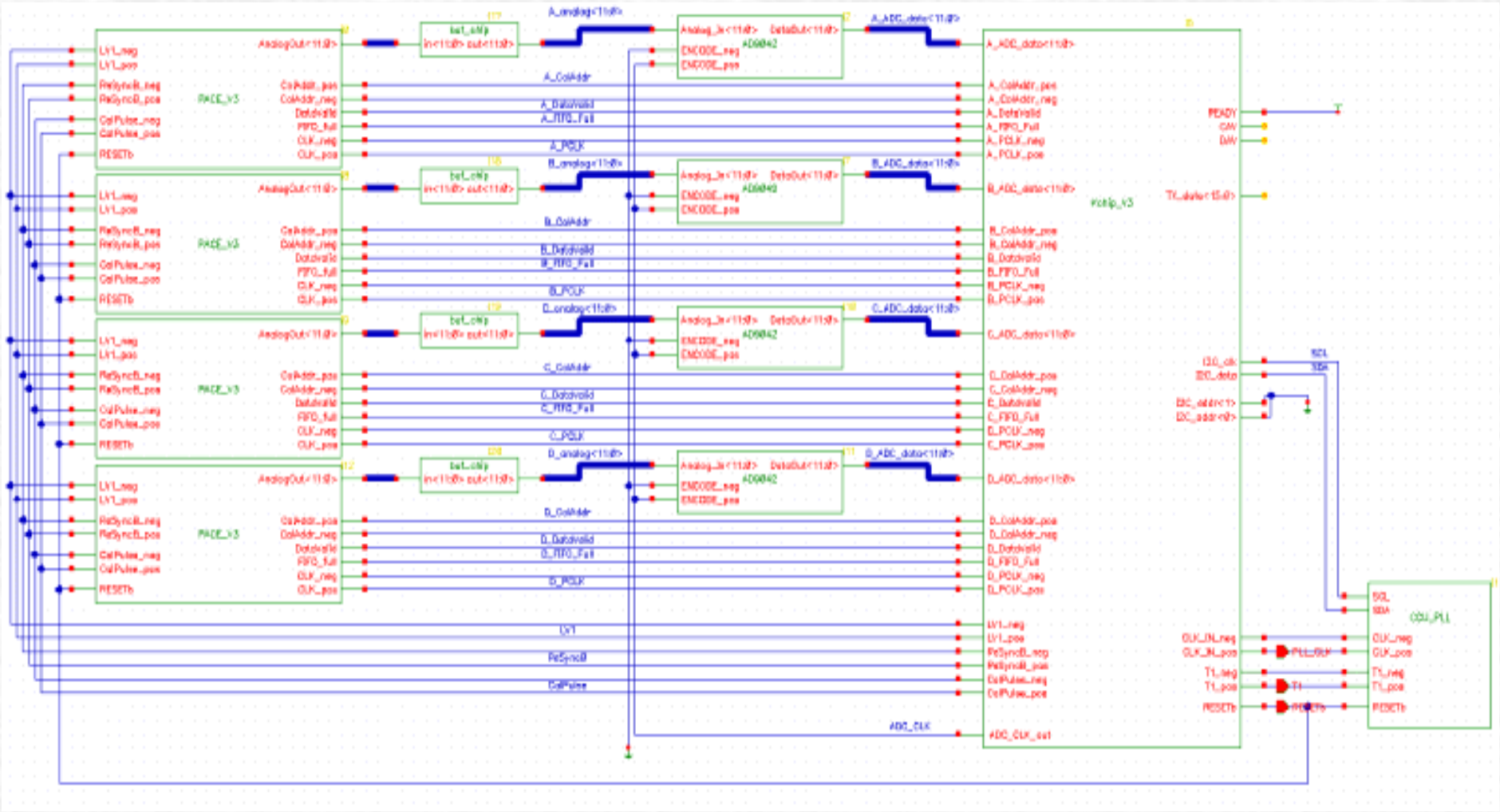


b)

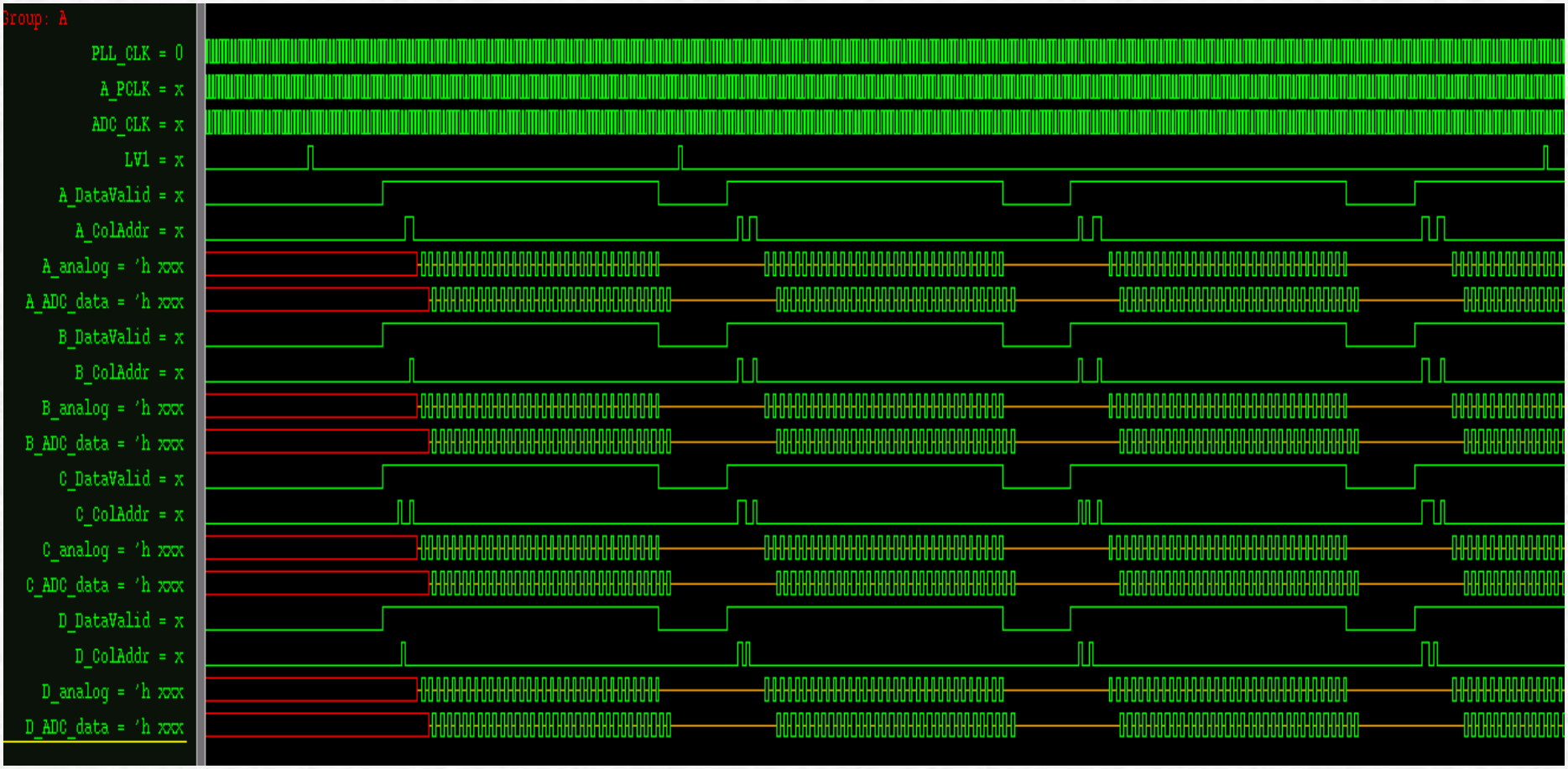


c)

FE System Test Bench



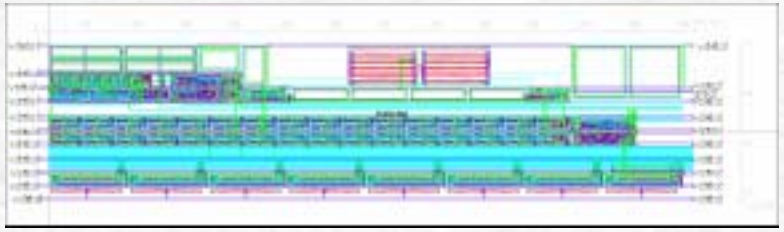
Readout of an Event



Calibration Circuit & DLL

- The Kchip delivers to the PACE3 chip a calibration pulse of programmable delay with respect to the system clock and with programmable width (1 – 256 cycles).
- The DLL from APV25 chip has been incorporated in the Kchip.
  - 16 steps of 3.25ns can allows for an offset of -9.75ns to +13ns from the rising edge of the calibration request signal.
- After an interval equal to the trigger latency a trigger is generated by the Kchip in order to readout the Calibration Event. (EC gets incremented upon a calibration event). This option can be disabled.

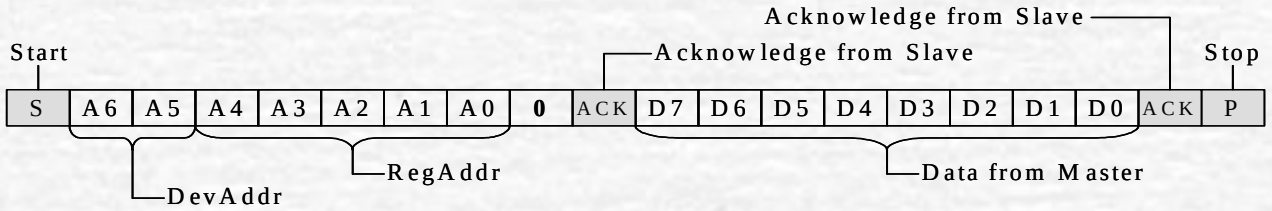
The DLL block as delivered from RAL.



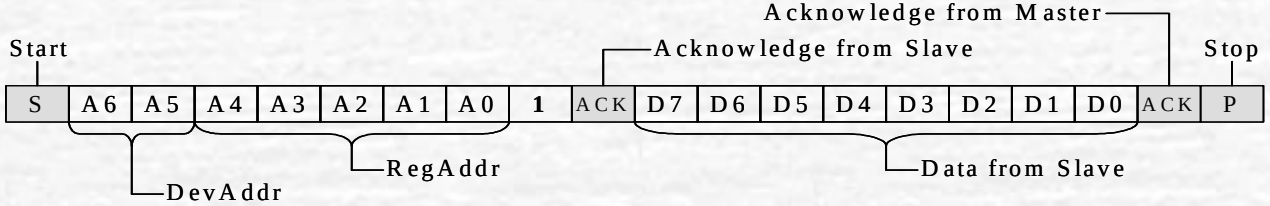
I²C Interface

- Follows the PHILIPS standard for 7-bit addressing Single Byte transfers
- Implemented using synchronous logic running with the 40MHz system clock. A synchronizer circuit is in use to avoid metastability problems on the SCL, SDA lines of the I²C bus..

Write Access



Read Access



Slave is the Kchip
Master is the CCU chip

I^2C Interface

- The I^2C interface can be used to access:
  - The Kchip internal registers.
  - The Kchip FIFOS
    (Data, Column Addr. and Trigger FIFOs).
- In Debugging mode the user
  - Can upload an event through the I^2C bus and then read it out through the High Speed Link.
  - Can readout an event through the I^2C bus.

Kchip Internal Registers

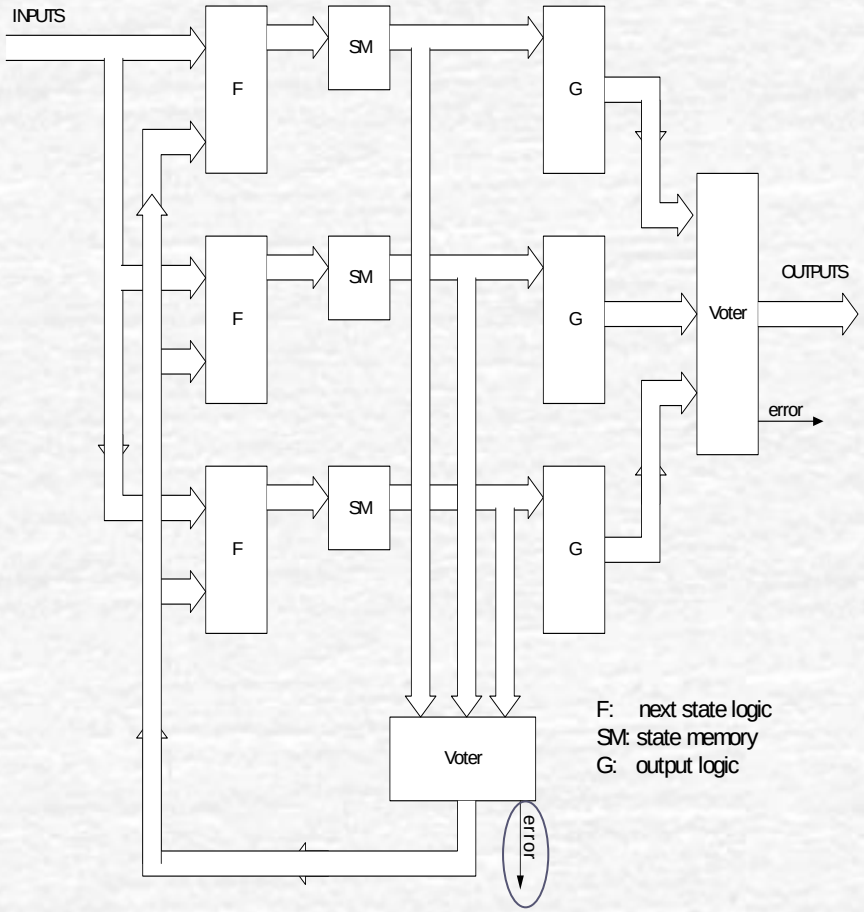
Name	I^2C Address	Function	Type
CONFIG	0	This register contains various configuration and mode fields as specified below. Default value: 8`b00001111	R/W
ECONFIG	1	This extra-configuration register contains various configuration and mode fields as specified below. Default value: 2`b00	R/W
KID_H-L	3-2	K-chip ID register. Default value: 16`b00000000000000xx	R/W
MASK_T1CMD	4	This register contains a 4 bit mask pattern for the Trigger Commands. Default value: 4'b0000	R/W
LAST_T1CMD	5	A read operation from this register returns the last issued Trigger Command.	RO
LATENCY	6	This register sets the Trigger Latency value, in clock cycles, for generating a readout cycle after a Calibration command has been issued. Default value: 'd128	R/W
EVCNT	7	A read operation from this register gives the 8 bit current content of the Event Counter in the K-chip	RO
BNCHCNT_H-L	9-8	A read operation from this register returns the 12 bit bunch counter value used to tag the last event.	RO
RESERVED	A		
GINT_BUSY	B	This register contains the timeout period for transmitting a synchronization pattern by the GOL interface. Default value: `d0	R/W
GINT_IDLE	C	This register contains the length of the synchronization pattern in the GOL interface. Default value: `d0	R/W
FIFOMAP	D	This register contains a pointer to one of the FIFOs in the chip, it is used to direct read/write operations to the corresponding FIFO	R/W
FIFODATA_H-L	E-F	When in Link Test mode, writing to this register causes data to be written into the FIFO pointed to by the FIFOMAP register; a read operation instead reads data from the corresponding FIFO. When in normal mode, read/write operations to this register are ignored.	R/W
STATUS_0	10	This register contains a number of status bits as specified below. It is reset upon a ReSync command.	RO
STATUS_1	11	This register contains a number of status bits as specified below. It is reset upon a ReSync command.	RO
SEU_COUNTER	12	This register contains the total number of single Events Upsets encountered on the chip since the last hardware RESET.	RO
CalPulse_DELAY	13	This register contains the delay period for generating a PACE calibration pulse. Default value: `d1	R/W
CalPulse_WIDTH	14	This register contains the width period of the PACE calibration pulse. Default value: `d1	R/W
RESERVED	15		
RESERVED	16		
RESERVED	17		
RESERVED	18		
RESERVED	19		
RESERVED	1A		
RESERVED	1B		
RESERVED	1C		
RESERVED	1D		
RESERVED	1E		
RESERVED	1F		

SEU Tolerant Techniques

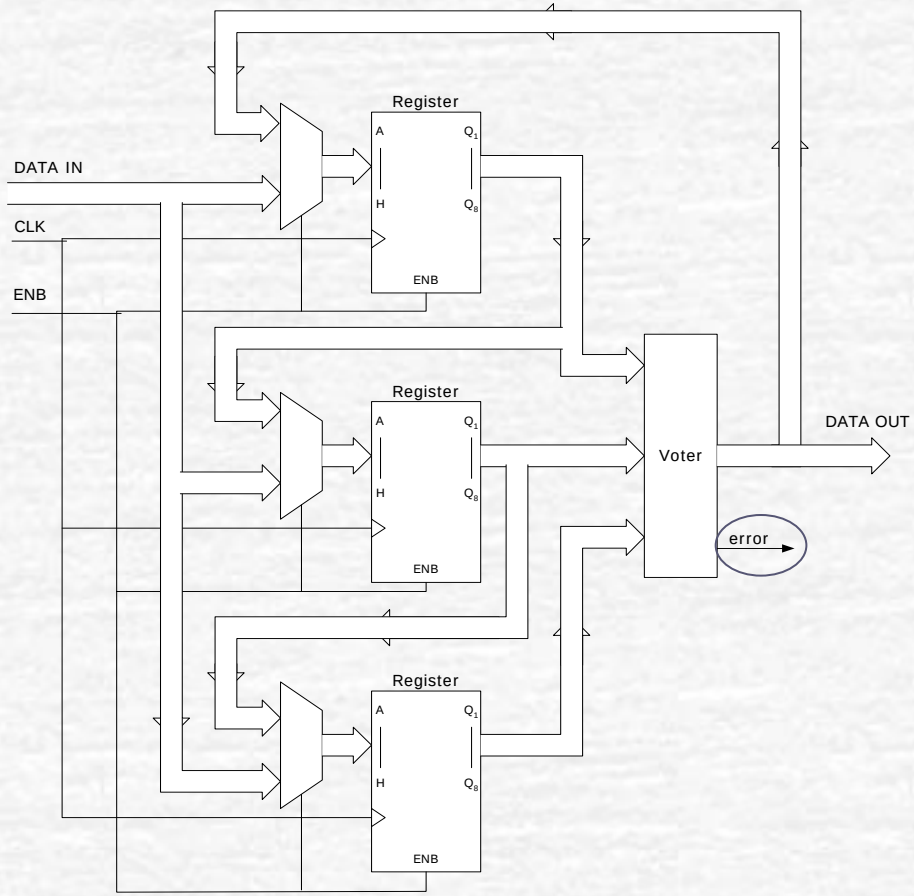
- Protect Control Logic using Triple Module Redundancy.
  - All State Machines and Configuration Registers have been triplicated.
- Leave Data Path unprotected.
  - SEU errors affect the integrity of small amount of information and does not lead to a loss of readout synchronization.

Triplicated Logic

State Machines



Configuration Registers



The Synthesized Chip

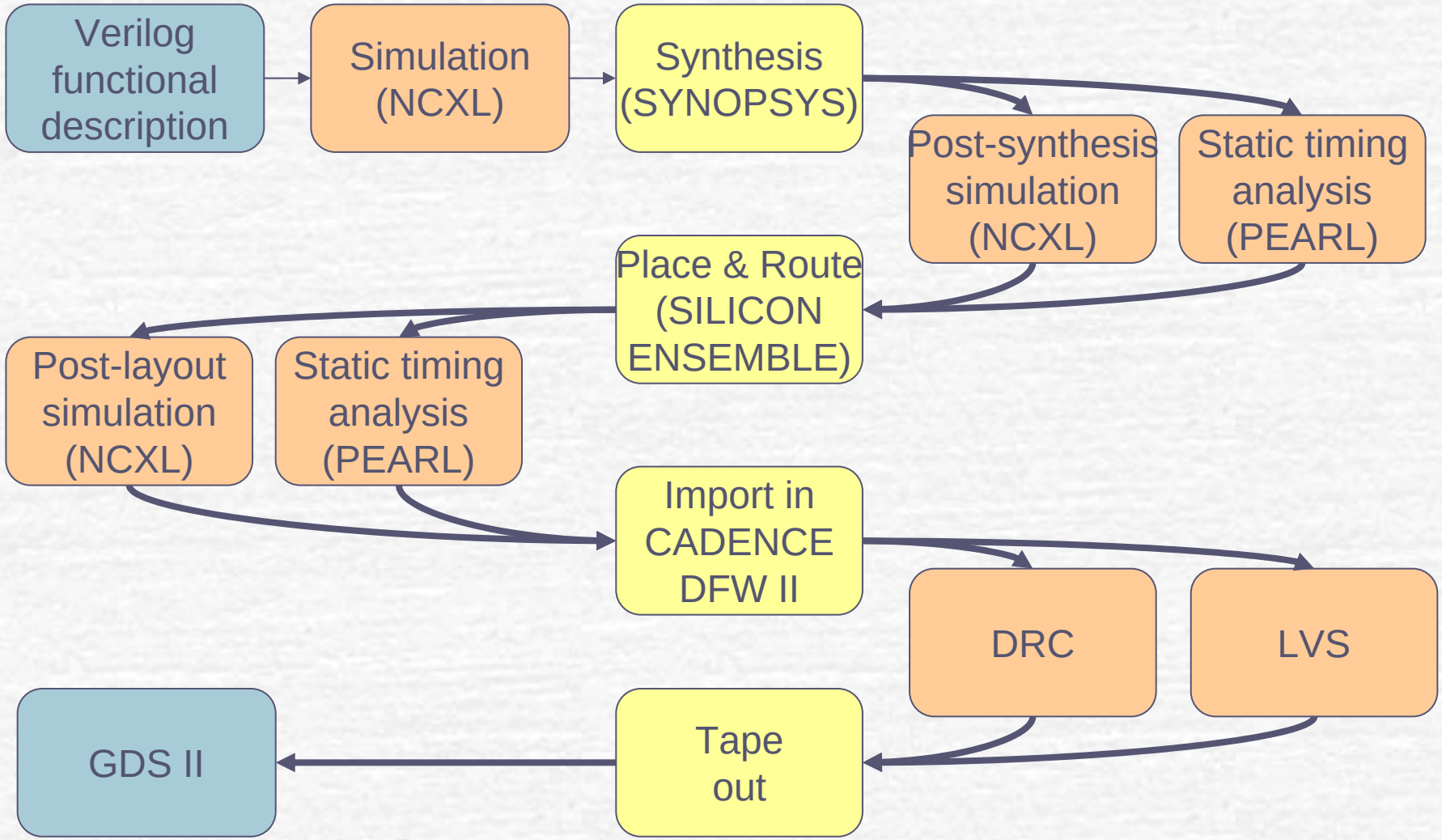
- Number of Digital Core cells
  - Without the Scan Patch
    - Registers: 1.3K
    - Gates: 11.4K
  - Including the Scan Path
    - Registers: 1.3K
    - Gates: 13K

  (This inventory does not take into account the clock tree buffers and the DLL logic block.)
- Number of pad cells
  - I/O pins: 131
  - Power pins: 17
  - Total pins: 148

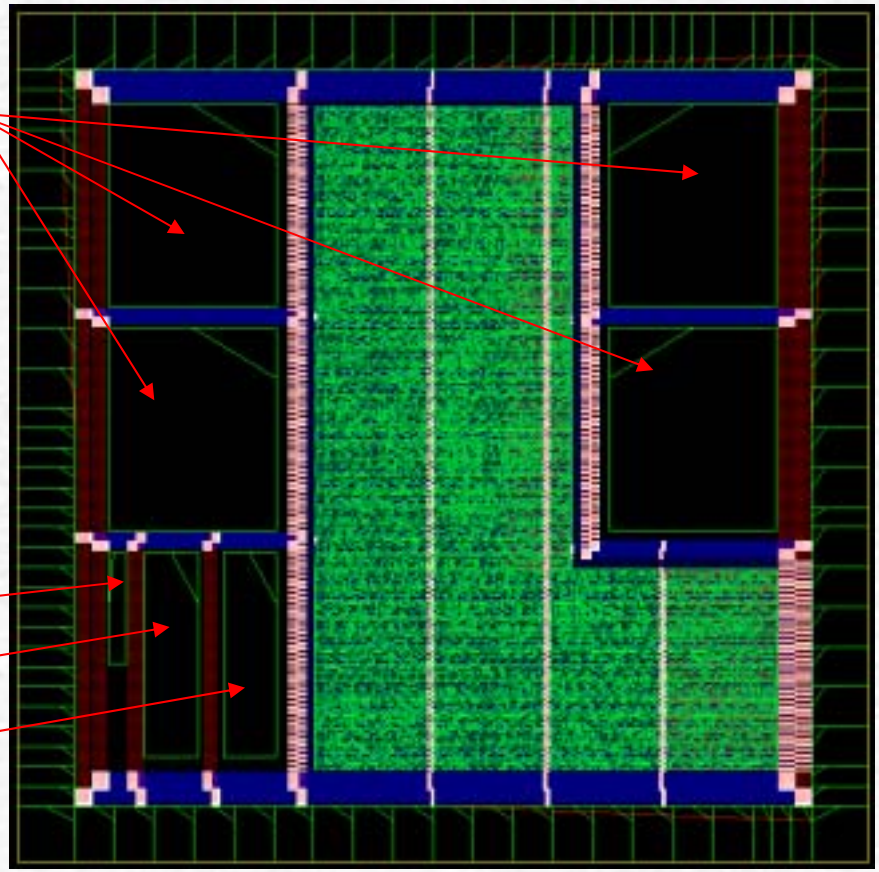
Design for Testability

- I^2C port
  - can be used to access and test the SRAMs
- Scan Path
  - For design debugging and production testing.
  - Scan Path clock uses the 40MHz system clock.
  - Shares I/O pins (+ 1 stand alone pin to enable/disable the scan mode).
  - Test vectors have been generated using “SYNOPSIS”. (1.7K vectors give 90% test coverage).

Kchip Design Flow



A *Preliminary* Layout



Size: 5.3 x 5.3 mm^2

Layout Considerations

- Is it foreseen to have a Preshower specific production run ?
- If yes, then a Preshower specific reticle should be assembled.
  - The aspect ratio of the Kchip layout should be decided taking into consideration the other Preshower chips.

- PACE: 6 x 5 mm^2
- DELTA:3.6 x 5 mm^2
- Kchip: 6 x 6 mm^2 should be changed to 5 x 7 mm^2 ?

Status & Planning

- Design Status
  - Preliminary version of the layout.
- Still To Do
  - Rerun FE System simulations using the synthesized version (gate level) of the PACE sequencer.
  - Back annotate any changes emerging from the design review into the chip design.
  - Final iteration through all the chip design steps. (script based operation)
- Schedule until Feb. 10, 2003
  - 1 week for the above mentioned items
  - 2 weeks for design verification.