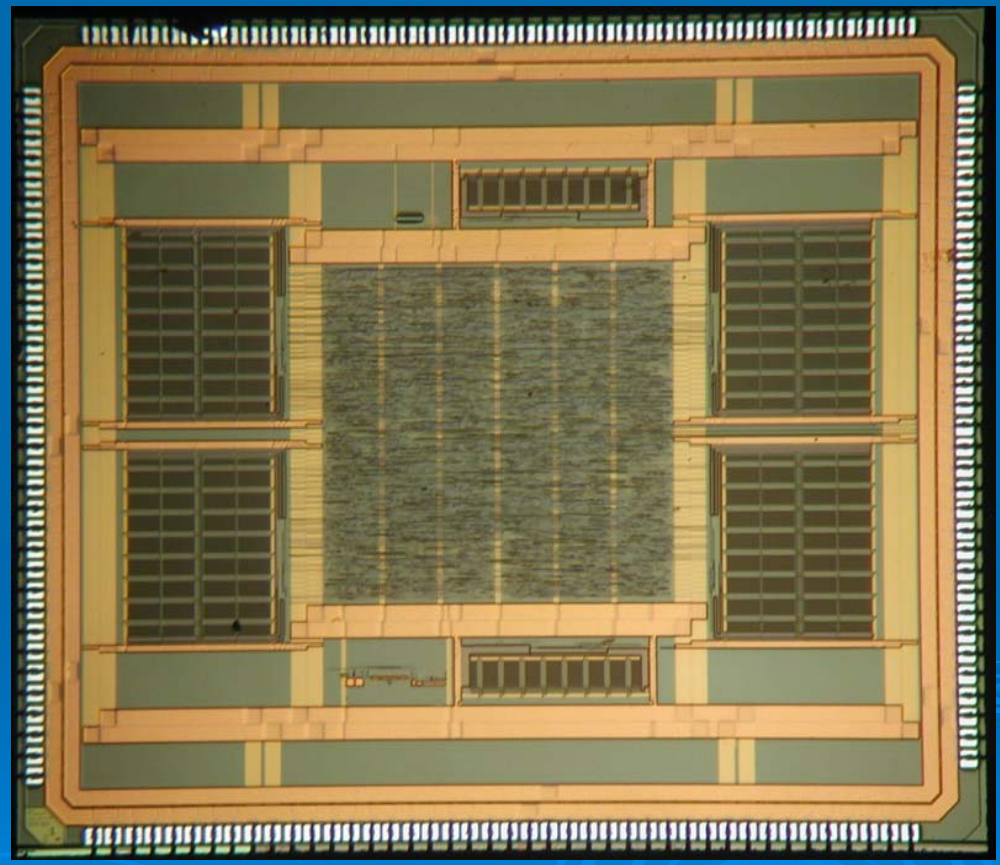
Testing the Kchip

Preshower Electronics Meeting

28/07/2003

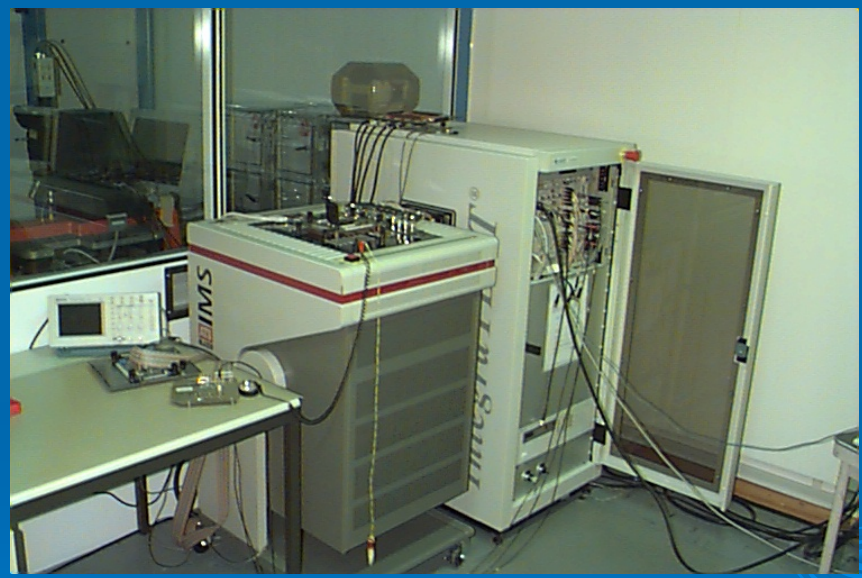
Testing the Kchip

- Functional Tests
- Irradiation Tests
- In System Tests

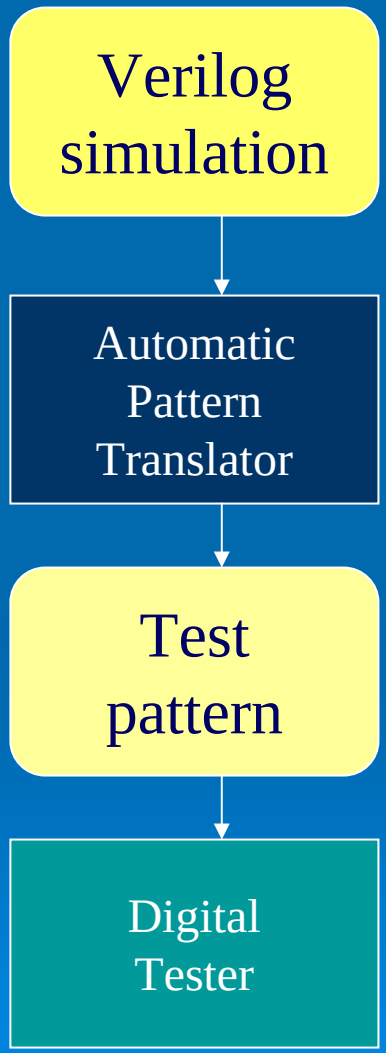


Functional Tests

- Scope
  - Test functionality & validate specifications conformity.
- Method
  - Make use of the in-house Digital Tester.
  - Use a generic “Test Fixture” to host the chip.
  - Use a ceramic package (CPGA) and in-house bonding.
  - Use “Test Vectors” from the simulation tool.

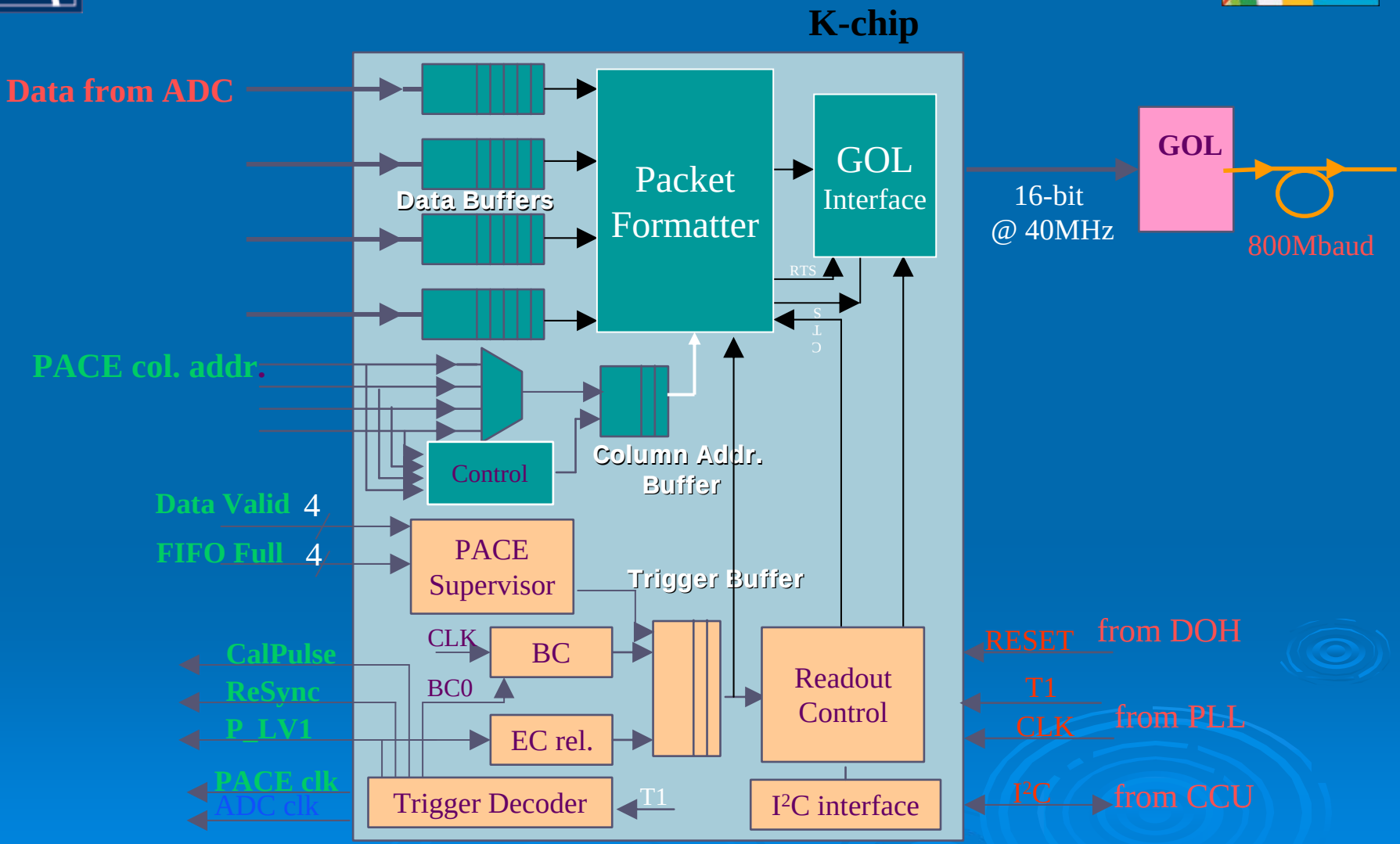


Functional Tests procedure



- A pattern translation tool automatically generates test pattern sequences from the Verilog simulation results
- The test pattern sequences are applied to the device under test by a digital tester equipment (ATS 200)
- The digital tester compares the device outputs with their expected value obtained from the Verilog simulation

Block Diagram



Functionality Tests

- I^2C interface
  - Successful tests on the digital tester.
  - I2C interface maximum speed: 3.33 Mbit/s
  - Successful Kchip communication with CCU.
    - 40MHz clock coming from the CCU board.

- Trigger Decoder
  - Decoding back to back commands.
  - Trigger Inhibit Logic.

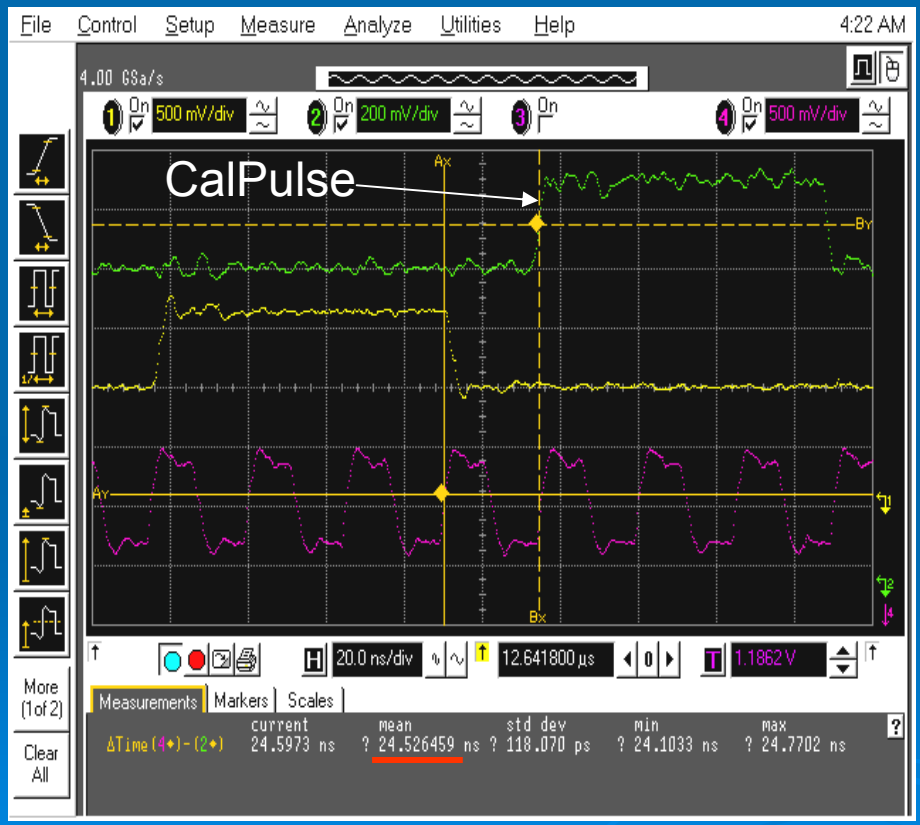
- Readout of Fuse bits

- Calibration Event Generation Logic
  - CalPulse Generation
  - Programmable CalPulse Timing (on chip DLL)

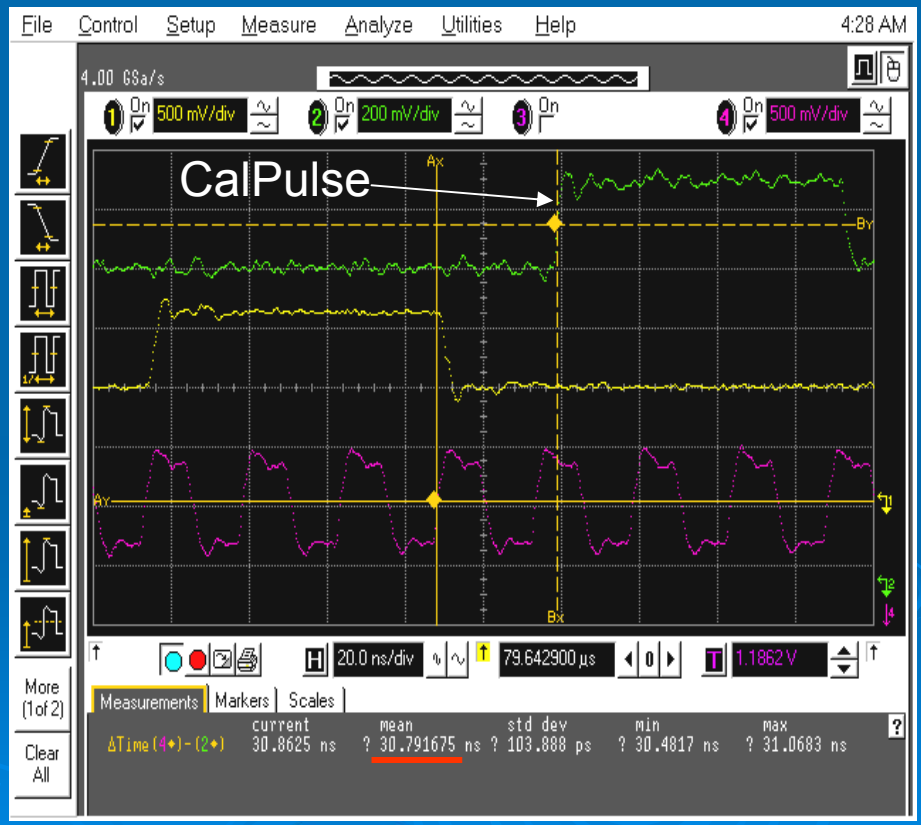
Testing the DLL

Test: Varying the CalPulse Delay

1st tap



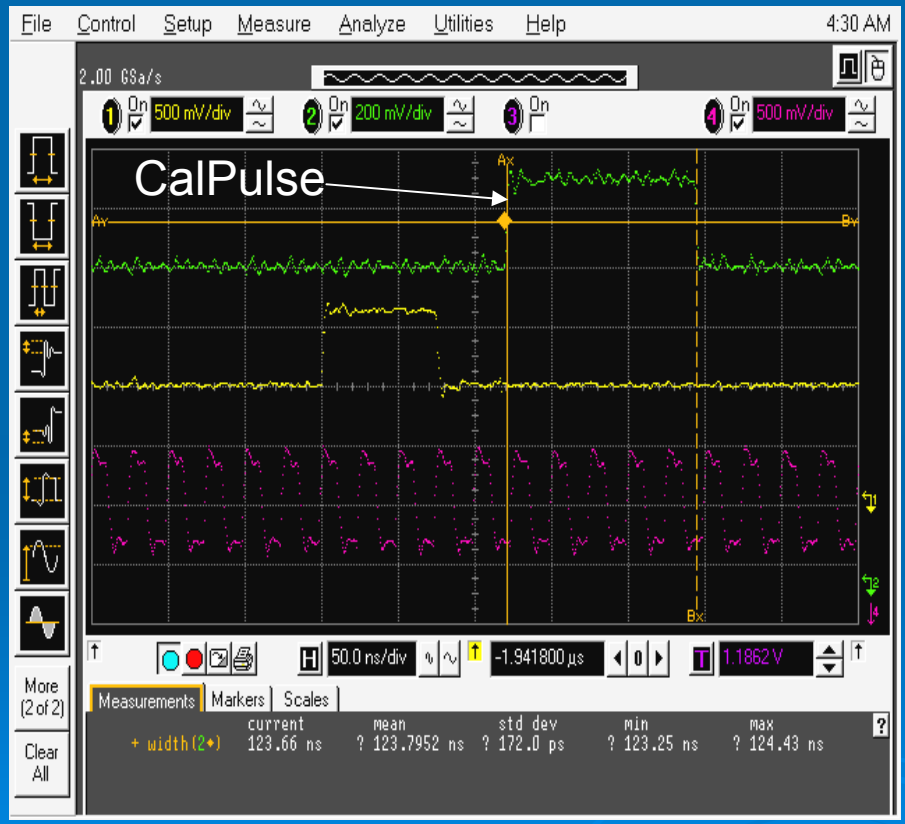
3rd tap

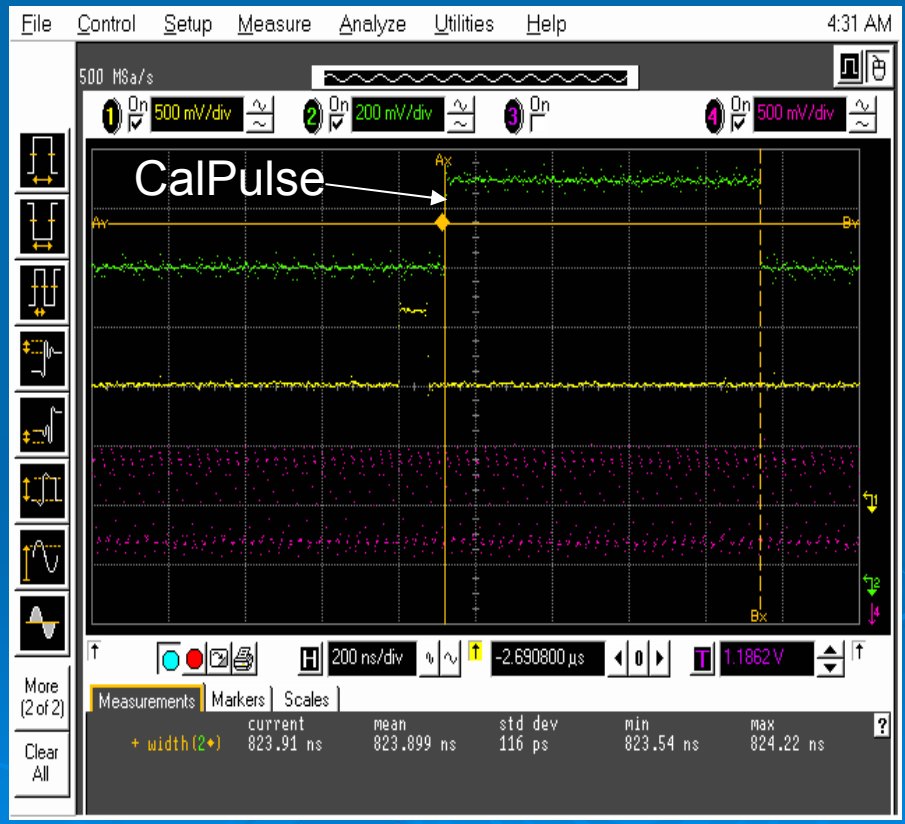


Incremental delay: 3.13 ns / tap

Testing the DLL

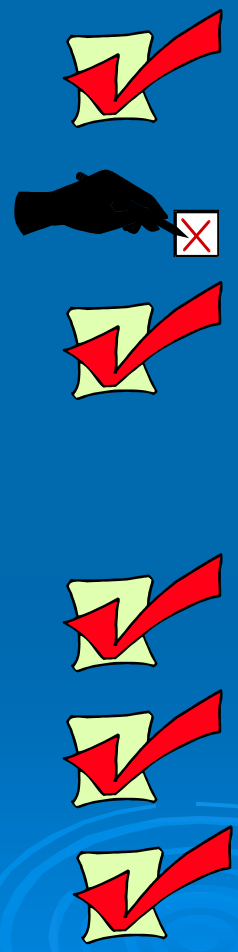
Test: Varying the CalPulse Width



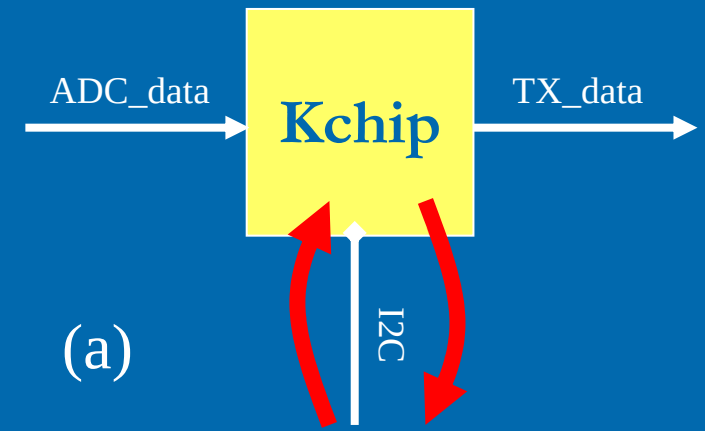


Functionality Tests

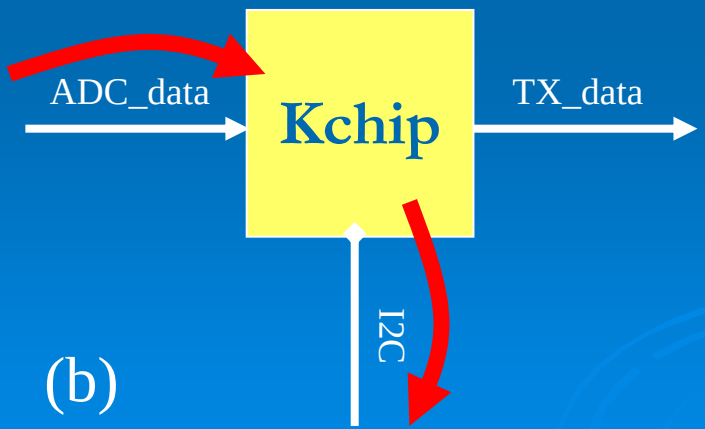
- Kchip in Normal Mode
  - Normal Readout
    - Packet Formatter & GOL interface.
    - Some Packets contained errors in data field.
  - Exception Handling
    - Kchip Data FIFO overflow.
    - Kchip Trigger FIFO overflow.
    - PACE Trigger FIFO Overflow.
    - PACE out of Sync.
  - Link Test Mode
    - GOL interface features
- SEU counter: No errors observed.
- Kchip in Test Mode
  - Access Data, Column & Trigger FIFOs from I^2C.



Test pattern sequences (1)

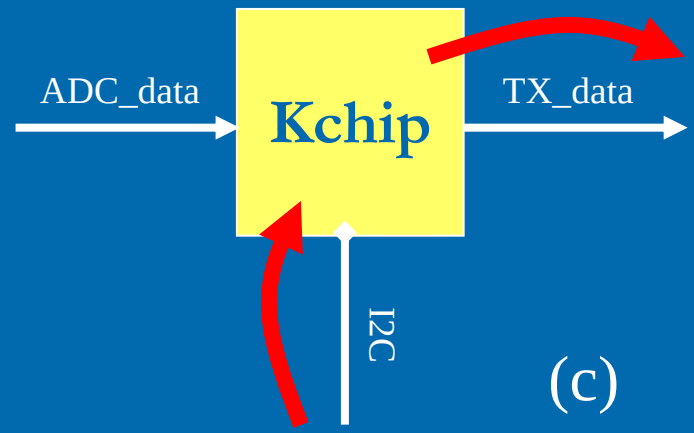


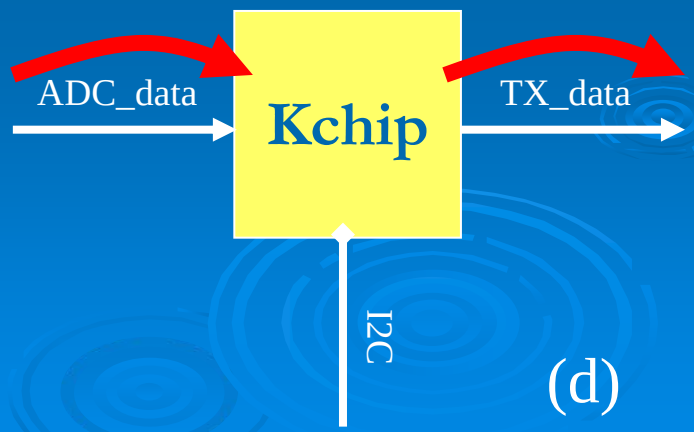
- (a) I2C read/write to the FIFOs and to the internal registers
- (b) Filling in the FIFOs from the ADC input bus and then reading data back through I2C interface



Test pattern sequences (2)

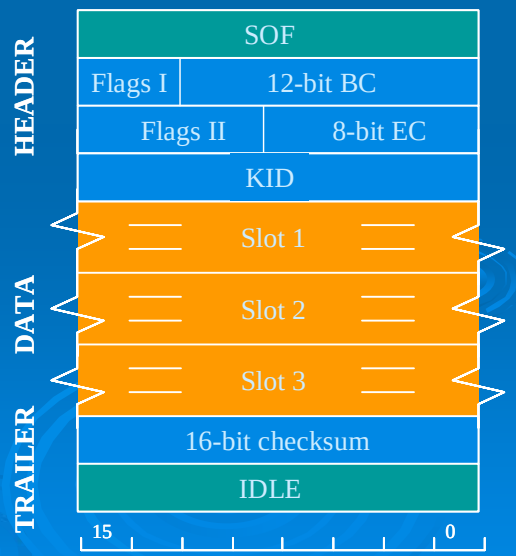
- (c) Loading data into the FIFOs through the I2C interface and then reading it out from the GOL output bus
- (d) Normal operation of the circuit, verifying the response in case of FIFO overflow





Errors in Data Packets

- Observations
  - Errors are seen only in the DATA field.
  - Error rate ~ 1event/100 triggers @100KHz exponential trigger rate.
  - Error rate increases with the trigger rate.
  - CRC is computed correctly on the erroneous data!
    - => DDU will see a packet with matching CRC!
    - => Errors are generated before the GOL interface.
- Error Rate depends on:
  - Process
    - Different chips give different number of errors.
  - Temperature
    - At lower temperature fewer errors.
  - Voltage
    - At lower voltages fewer errors
  - => indication of signal race condition.



Error in data packets

- Use of Scan Path excluded errors in the standard logic blocks.
- Use I^2C to test Data FIFOs
  - => errors are generated in the SRAMs
- Errors are “traffic” dependent
  - If Write only and then Read => No Errors
  - If Write followed by Read => Errors possible
  - Errors are seen for specific combinations of WA (Write Address) and RA (Read Address) pointers.

Errors in Data Packets

- Generated special test vectors to produce the following traffic:
  - Send a number of triggers spaced at 6.9μs (PACE readout time) to establish a difference between WA and RA pointers.
  - Send hundreds of triggers spaced at 7.475 μs (Kchip service time) to maintain the pointers difference through out the test.

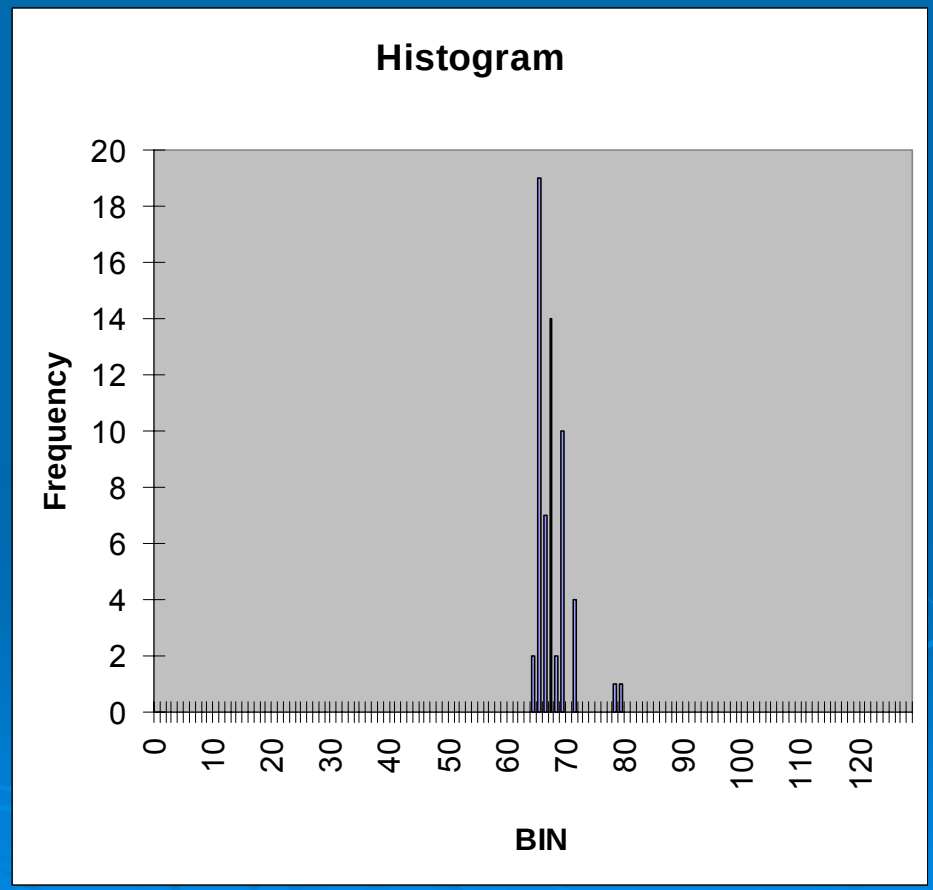
- Error generation is more pronounced when the difference between the WA and RA pointers is ~64 locations !
  - Indication that the error comes from the address decoding of the 6 lower bits
  - Possible causes:
    - problem in wordline decoder of the SRAM
    - Interface problem with the FIFO controller.

WA - RA	errors
0	0
56	210
63	924
70	373
129	0
199	903

Errors in Data Packets

- Correlation between two consecutive WA - RA addresses.

- Generated special test vectors to produce random traffic @ 100KHz rate:
  - Perform the XOR function on the WA and RA pointers.
  - Fold back addresses beyond 128 (range of wordline decoder).
  - Produce histogram.
  - Errors are localized around 64.
  - => bit A6 is not decoded correctly



Errors in Data Packets

RA[6:0]	WA[6:0]	RA[6:0]	WA[6:0]	xor
2D	6C	0 1 0 1 1 0 1	1 1 0 1 1 0 0	1 0 0 0 0 0 1
2E	6F	0 1 0 1 1 1 0	1 1 0 1 1 1 1	1 0 0 0 0 0 1
2F	6C	0 1 0 1 1 1 1	1 1 0 1 1 0 0	1 0 0 0 0 1 1
2F	6E	0 1 0 1 1 1 1	1 1 0 1 1 1 0	1 0 0 0 0 0 1
30	71	0 1 1 0 0 0 0	1 1 1 0 0 0 1	1 0 0 0 0 0 1
31	70	0 1 1 0 0 0 1	1 1 1 0 0 0 0	1 0 0 0 0 0 1
31	72	0 1 1 0 0 0 1	1 1 1 0 0 1 0	1 0 0 0 0 1 1
32	72	0 1 1 0 0 1 0	1 1 1 0 0 1 0	1 0 0 0 0 0 0
32	73	0 1 1 0 0 1 0	1 1 1 0 0 1 1	1 0 0 0 0 0 1
33	70	0 1 1 0 0 1 1	1 1 1 0 0 0 0	1 0 0 0 0 1 1
33	72	0 1 1 0 0 1 1	1 1 1 0 0 1 0	1 0 0 0 0 0 1
33	7D	0 1 1 0 0 1 1	1 1 1 1 1 0 1	1 0 0 1 1 1 0
34	75	0 1 1 0 1 0 0	1 1 1 0 1 0 1	1 0 0 0 0 0 1
34	77	0 1 1 0 1 0 0	1 1 1 0 1 1 1	1 0 0 0 0 1 1
35	70	0 1 1 0 1 0 1	1 1 1 0 0 0 0	1 0 0 0 1 0 1
35	74	0 1 1 0 1 0 1	1 1 1 0 1 0 0	1 0 0 0 0 0 1
36	75	0 1 1 0 1 1 0	1 1 1 0 1 0 1	1 0 0 0 0 1 1
36	77	0 1 1 0 1 1 0	1 1 1 0 1 1 1	1 0 0 0 0 0 1
37	72	0 1 1 0 1 1 1	1 1 1 0 0 1 0	1 0 0 0 1 0 1
37	74	0 1 1 0 1 1 1	1 1 1 0 1 0 0	1 0 0 0 0 1 1
37	76	0 1 1 0 1 1 1	1 1 1 0 1 1 0	1 0 0 0 0 0 1
38	79	0 1 1 1 0 0 0	1 1 1 1 0 0 1	1 0 0 0 0 0 1

Errors in Data Packets

- Problem is located
  - in the decoding function of the lower part of the addresses in the SRAM modules that are used to implement the Data FIFOs.
- Fixes
  - Increase fan-out strength of standard cell login of the FIFO controller.
  - Layout of SRAM module needs revision.
    - Routing of the wordline decoder address bus.

Power Consumption

- Measurements (VDD= 2.5V)
  - I_{peri} = 182mA, P_{peri} = 455mW
  - I_{core} = 68mA, P_{core} = 170mW
  - I_{total} = 250mA, P_{total} = 625 mW
- Simulations
  - Pcore = 200mW
  - Pperi
    - $LVDS_{RX}$ 32 x 6.9mW = 221mW
    - $LVDS_{TX}$ 17 x 10.4mW = 177mW
    - $R_{term.}$ 17 x 1.2mW = 21mW
    - P_{total} = 419mW

Irradiation Tests

- Total Dose tests
  - Use the X-ray machine to reach 20MRad
  - The “Test Fixture” board was used for the irradiation test.
  - Step Irradiation of one chip at 1, 3, 5, 10, 20 MRad.
    - Chip was functional up to 20MRad @ 2.5V, 40MHz.
    - Observed a *slight drop in power dissipation*.
      - $I_{pre\text{-}rad}$ = 283mA, I_{10MRad} = 272mA => ΔI = 2%
- SEU tests
  - Make use of the FE system motherboard.
  - SEU tests could be scheduled in common for all our FE electronics chips (PACE, ADC, Kchip)
  - SEU tests are very important and should be scheduled very early.
  - Evaluated results are needed before the *next submission* of the chip.

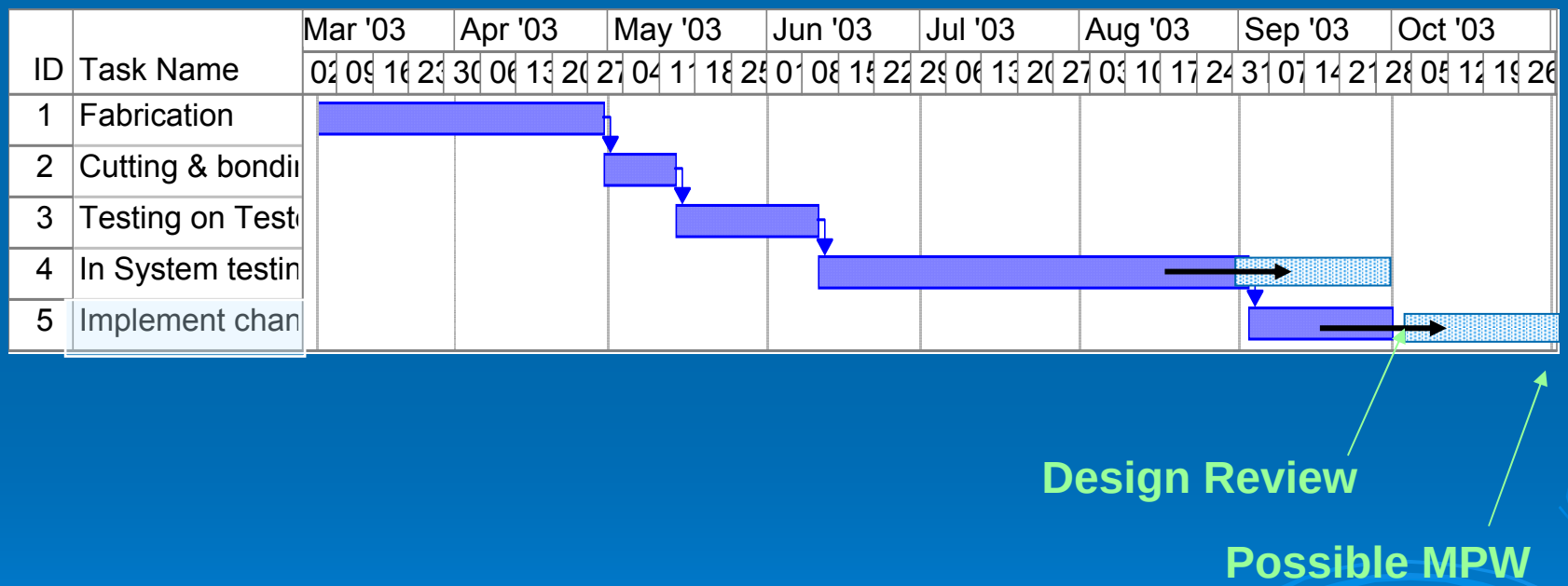
In System tests

- Scope
  - Integration of the Kchip on the “Preshower FE system motherboard”
    - Verify the Kchip interfacing with the PACE_AM, ADC and control (QPLL, TPLL, CCU) chips.
    - Evaluate the Kchip in-system functionality.
- Planning
  - Packaging on the fpPGA
    - Revised the bonding scheme to facilitate LVDS signal routing.
    - Packaging of 144 chips has been ordered.
    - Customized test-board for the Digital Tester (PCB layout in process). This board can be used for production testing.
  - Work with Serge
    - Help in the motherboard design for hosting the Kchip.
    - Help in the system tests.

Next Run Wish List

- Mandatory
  - Fix Data FIFO SRAM.
  - Extend the fuse bits from 16 to 24.
  - I^2C I/O pads with hysterisis.
- Provisional
  - Protect Data FIFOs using Hamming Encoding.
  - BIST (Built In Self Test) for the FIFOs.
  - Divide the scan path to reduce production testing time.
    - 1 scan path chain results in ~ 6min of test time. (Present)
    - 5 scan path chains results in ~ 1 min of test time.
- Not yet known
  - Input needed from In System Tests !

Planning


ID
Task Name
Mar '03
Apr '03
May '03
Jun '03
Jul '03
Aug '03
Sep '03
Oct '03
1 Fabrication
2 Cutting & bondi
3 Testing on Test
4 In System testin
5 Implement chan
Design Review
Possible MPW