Preshower - CMS Synchronization Issues

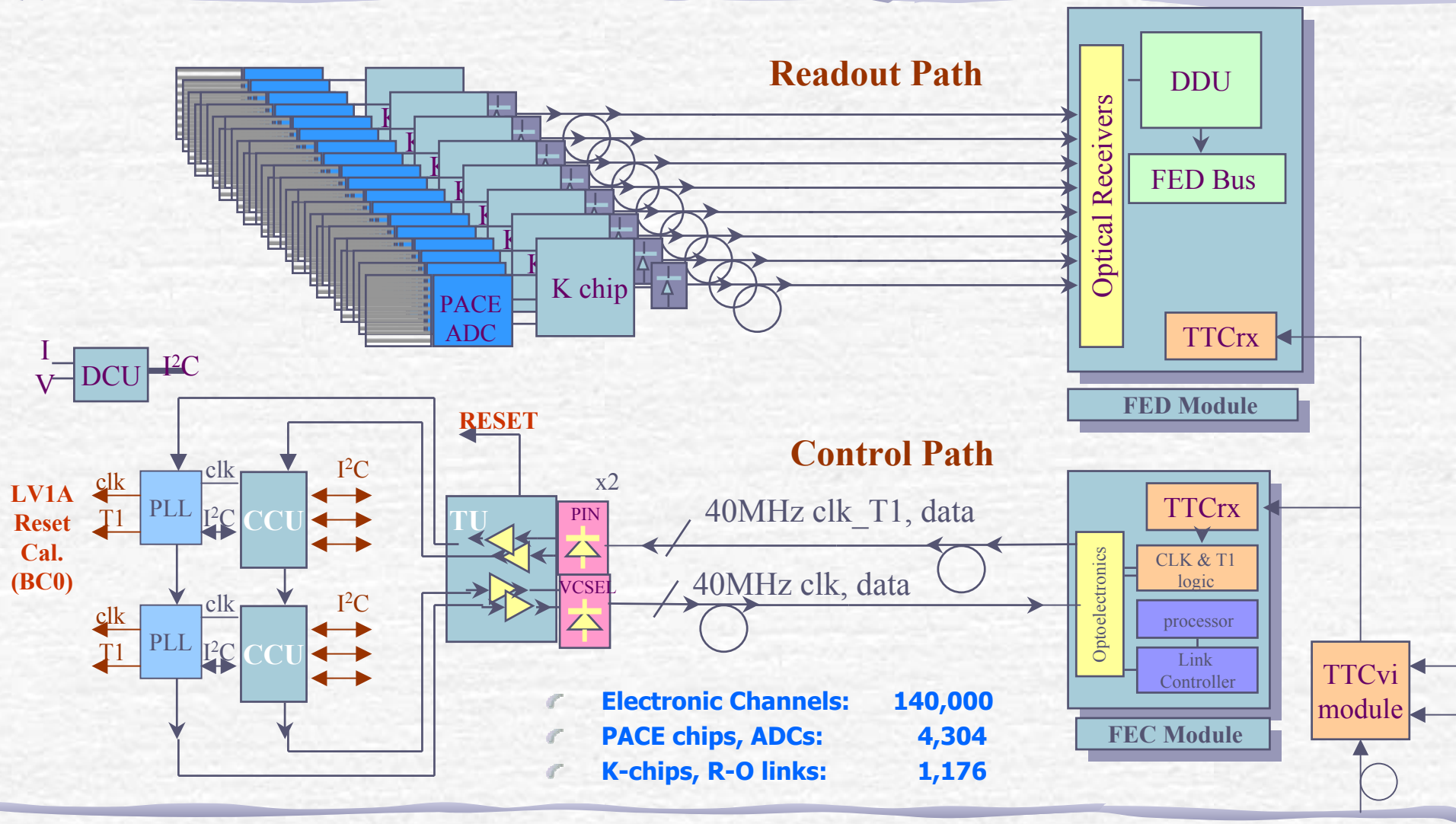
This presentation is the response to the *CMS Synchronisation Document* on behalf of the CMS Preshower

Issues covered:

Preshower Readout and Control Architecture

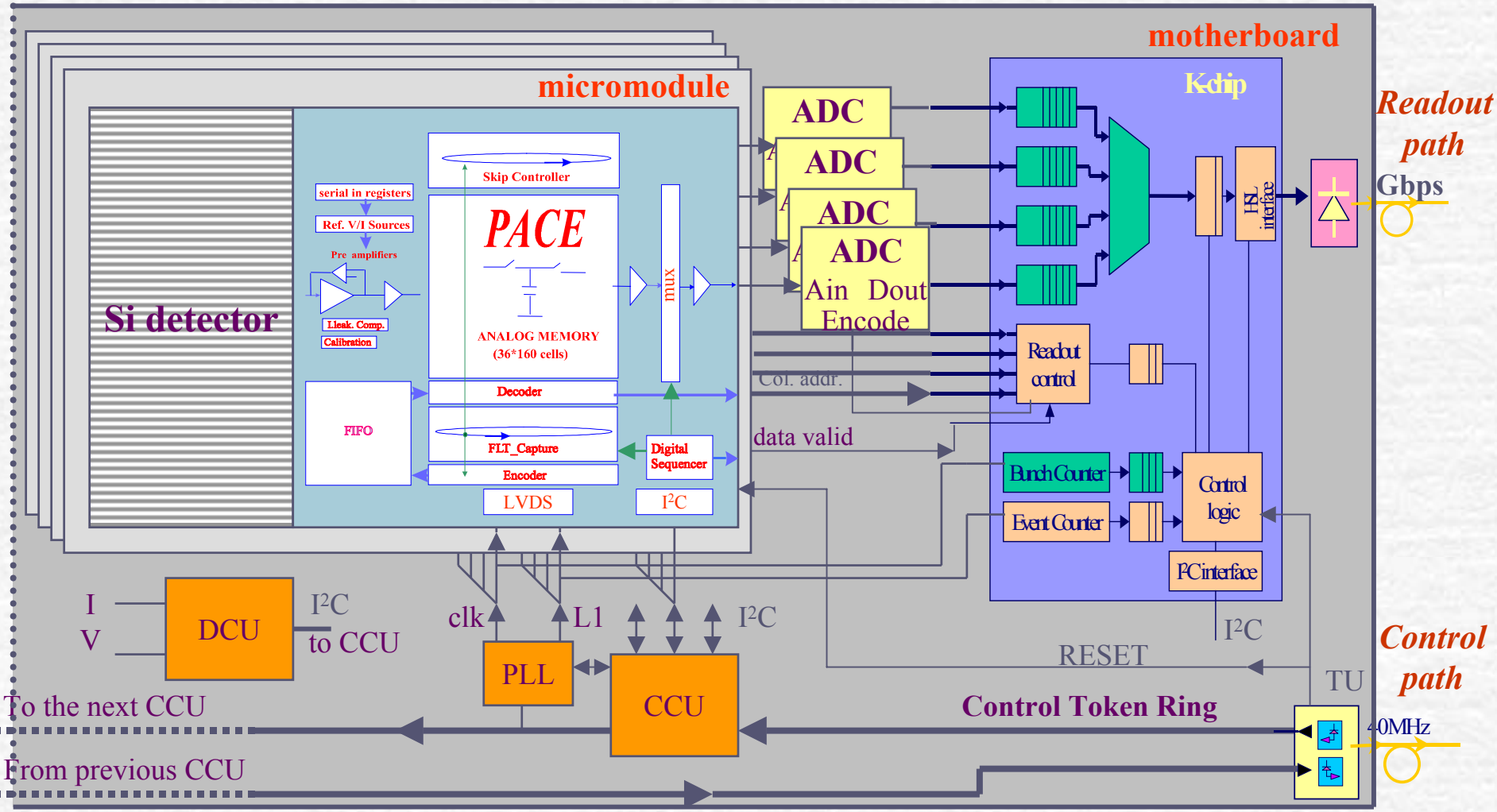
Sub-Detector Synchronisation

General Readout & Control Architecture



- **Electronic Channels: 140,000**
- **PACE chips, ADCs: 4,304**
- **K-chips, R-O links: 1,176**

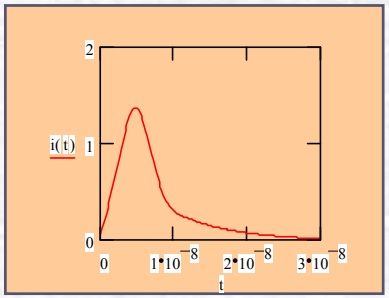
Preshower Readout & Control Front-End Electronics

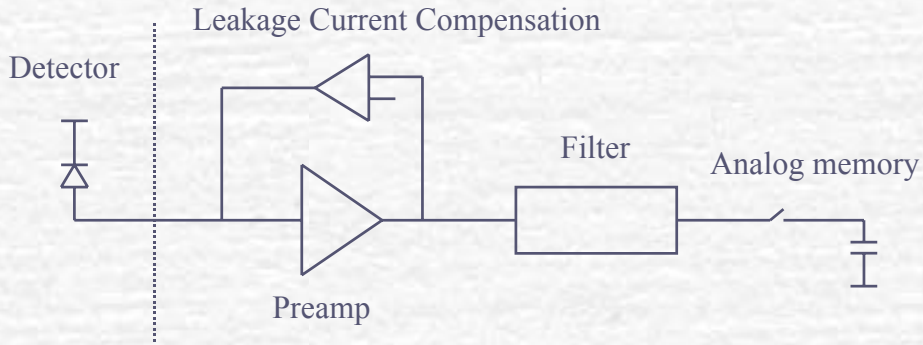


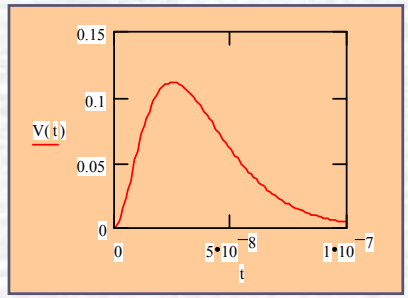
Detector Signals
Timing characteristics

*6cm * 2mm Si strips (pads)*
300μm thick, producing ~ 4fC / mip

Signal response linear over 400 mips







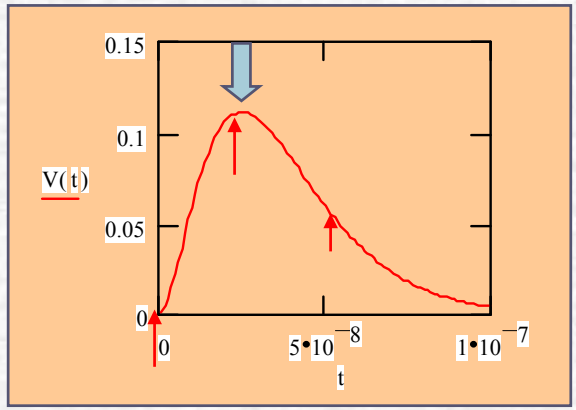
- *Rise time : 5 ns (electrons)*
- *The signal decreases to about 1/5 of it's maximum value at 10ns*
- *The signal then gently decreases linearly to zero which is reached around 25 ns (hole collection)*

Detector Signals Synchronisation Issues

Synchronization of detector signals with 40MHz clock

** Particle "time of flight" corresponds to approx. 1ns across the Preshower.*

** The PLLs are grouped in rings of about 8, each one inserting a delay on the clock. A timing curve would be done for each region adjusting the phase of the clock for each PLL using particles to align peaks.*



Distribution of fast control signals

** The Preshower uses the tracker fast control distribution system.*
Hence : The FEC delivers the Clock, LV1A, Reset and Calibration signal through an optical link to the PLLs on the Front-End electronics. The PLLs then send both a 40MHz phase adjusted clock and a (LV1A, Reset, Cal) signal in LVDS to the Readout Front-End chips (PACE, K-chip).

Calibration and Test Triggers

- Since triggers in T+1 and T+2 are forbidden, we intend to use combinations of trigger patterns for various functions.
  - *1 0 0 … LV1A*
  - *1 1 0 … Test Pulse (calibration and alignment testing)*
  - *1 0 1… Reset*
  - *(1 1 1… BC0)*
- In calibration mode : A LV1A should therefore arrive after the test pulse signal with a delay equal to the LV1A latency + a few clock periods.

Clock phase adjustment and Jitter performance

Requirements for clock jitter

- The charge measurement accuracy of the Preshower is approx. 5%. Charge integration in 3 time slots insensitive to jitter at the ns level. Voltage sampling with 3 samples, 30ns peaking time -> simulations show a 1ns jitter from one sample to the next gives ~ 2% error. Hence a jitter < 1ns p.p. is tolerable.
- The operation of High Speed Links requires a low jitter clock.

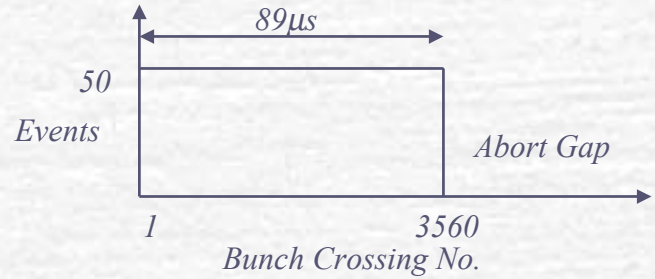
Requirements for clock Phase adjustments

- Preliminary simulations show that voltage sampling using 3 samples and a ±2ns phase variations has almost no impact on the charge measurement.
- The step size of the PLL is 1ns. This is good enough for the Preshower.
- The phase will be scanned in 1ns steps to correctly position detector pulses.
- We do not expect to have to adjust the clock phase often.

Bunch Crossing Identification

Bunch crossing identification and Clock Phase monitoring

Histogram method



Probability of a non-zero event at low luminosity ……. $3*10^{-3}$
Say 50 entries per bunch crossing,
3560 bunch crossing per 89us
We therefore need $6*10^{7}$ events > 800 s (with 75kHz LV1A)

This assumes :

* *Good S/N (High gain mode)*
* *Histogram at the full rate (75kHz)*
  either in the DAQ
  or by a μp in the FED (we would need a bunch crossing no. for each trigger).

Synchronization Procedure

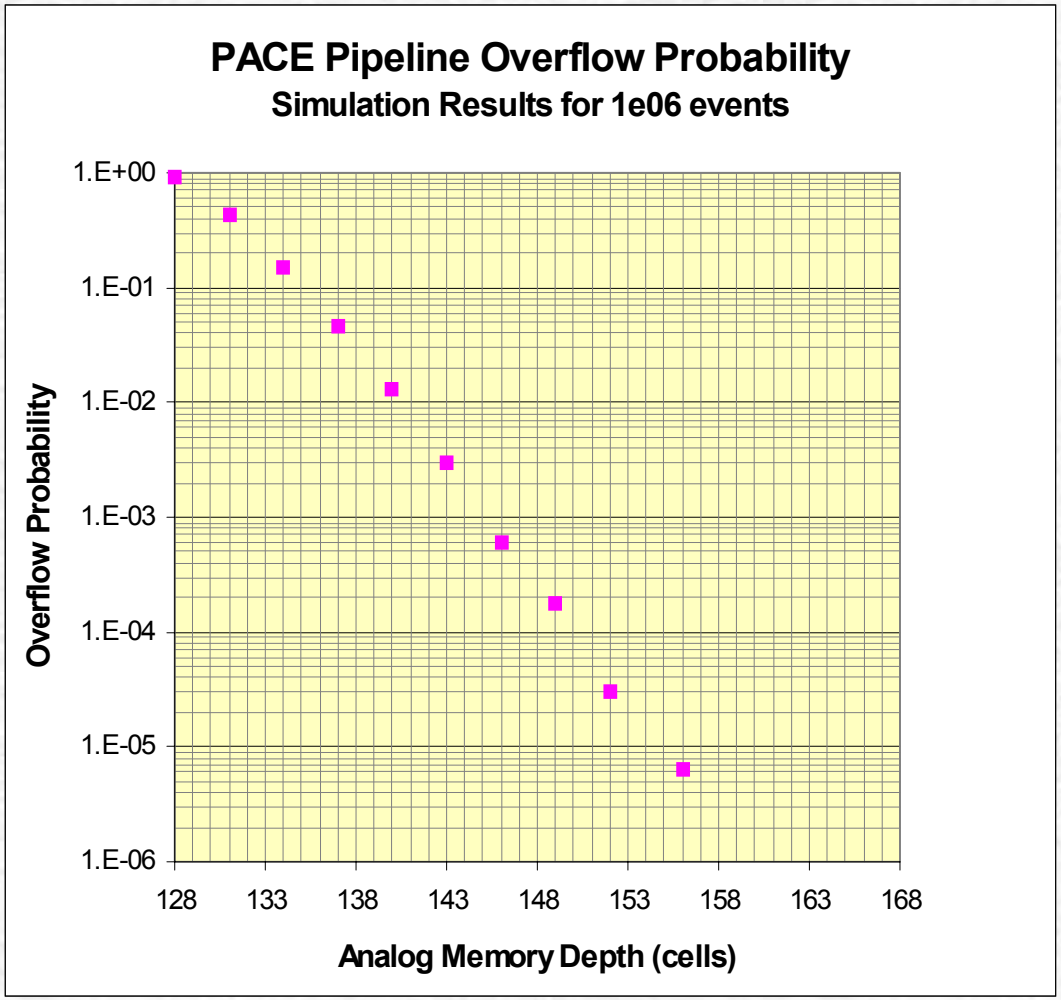
As above

Verification : Correlate a large energy deposition in the ECAL (a few GeV) with the Preshower

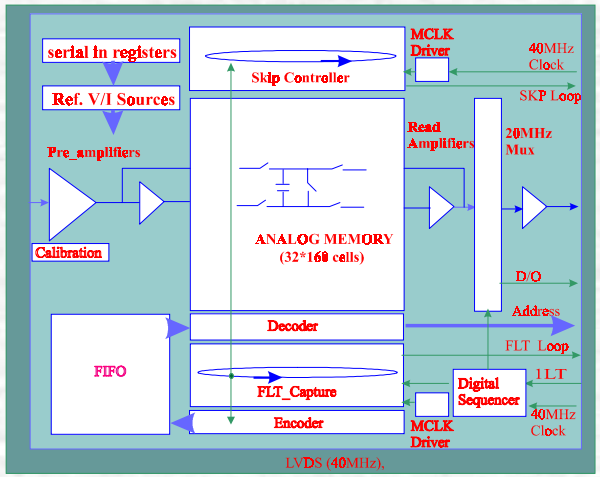
Front-End Pipeline - Derandomizer

- PACE
  - Voltage Sampling technique
  - Radiation Hard
  - 32 (+4) channels
  - 160 cells deep
  - 3 samples per Trigger
  - Programmable Latency
  - Calibration & biasing on chip
  - 24 words deep FIFO,
    hence up to 8 Triggers can be stored

Front-End Pipeline Overflow

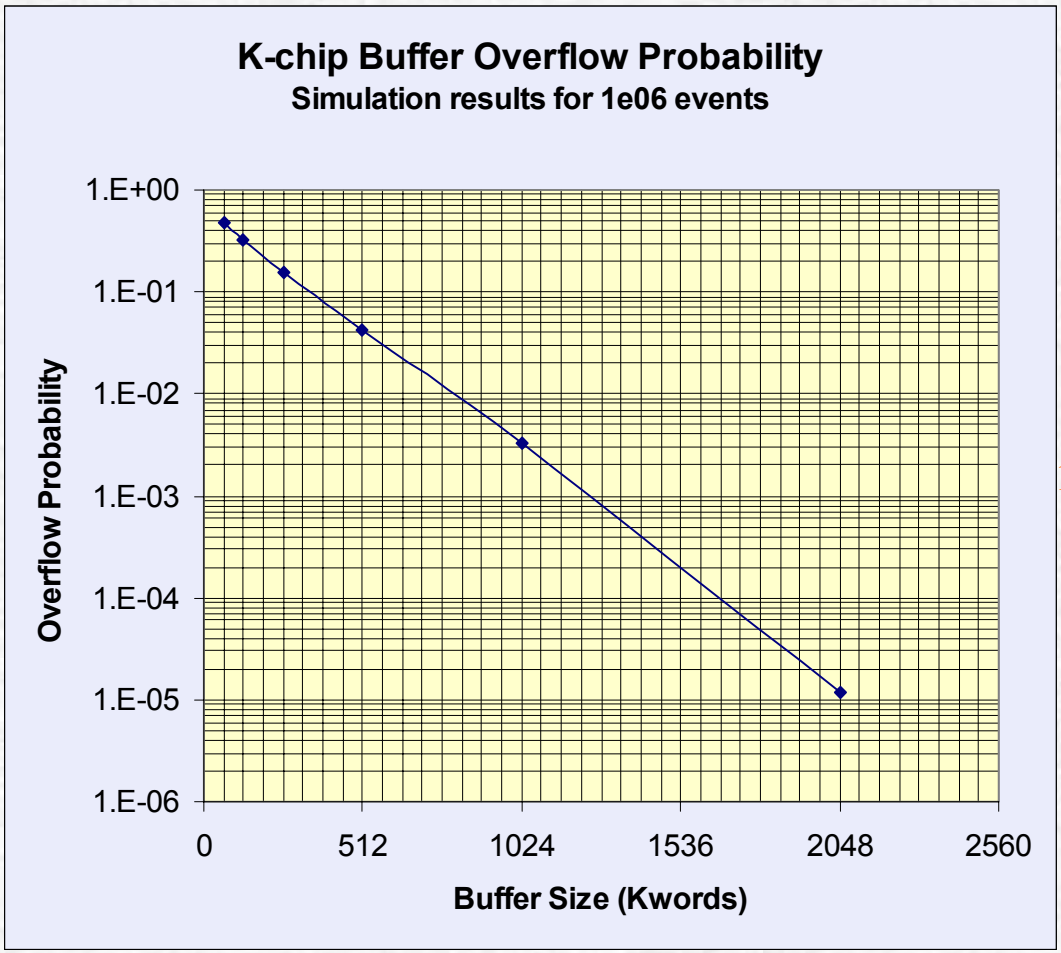


- Pipeline size
- Trigger Latency : 128 cells
- FIFO size : 8*3 cells
- Overhead : 8 cells
  = 160 cells
- *Overflow Probability: ~2e-06*

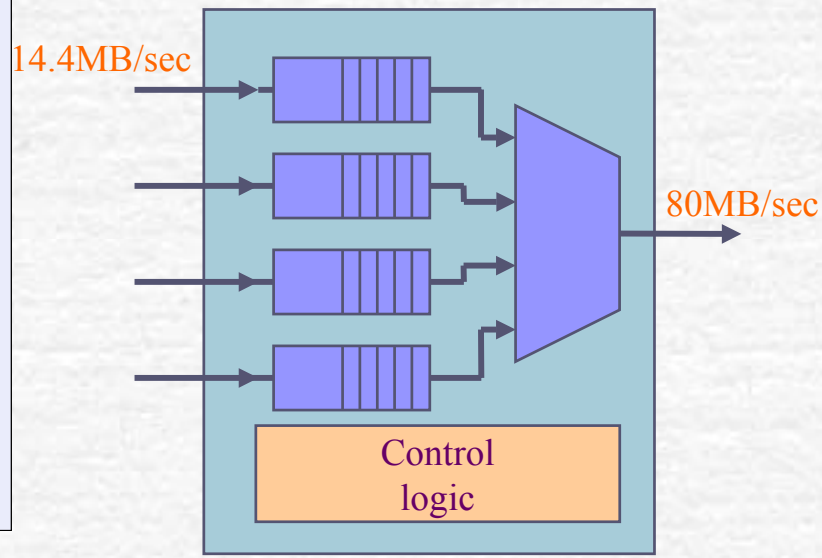


- Samples per Event: 3
- Channels MUXed in: 32
- Trigger Rate: 100KHz
- MUX Freq. : 20 MHz

Front-End FIFO Overflow



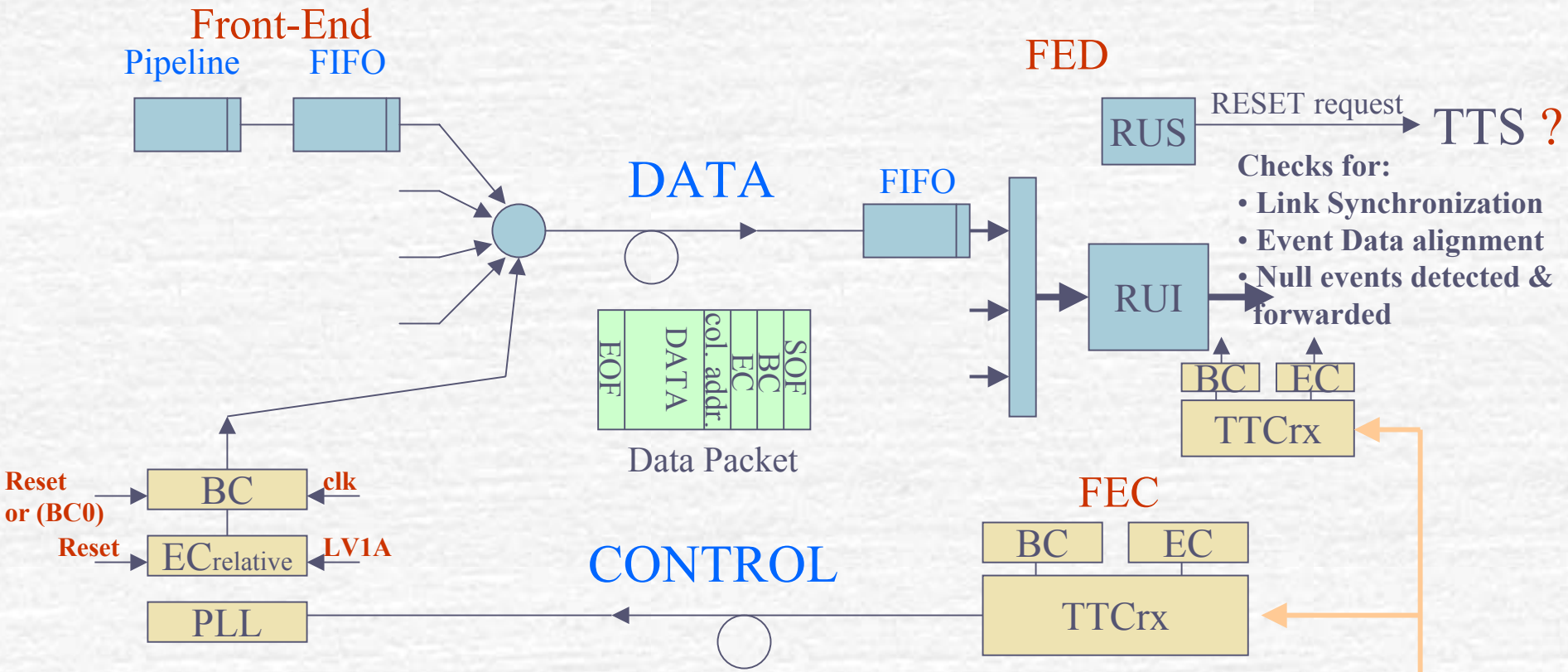
- Samples per Event: 3
- Channels MUXed in: 32
- Trigger Rate: 100KHz
- Link Throughput: 640Mbps



Buffer Overflow Handling

- Front-End PIPELINE (PACE chip)
  - Trigger Inhibit Logic on the Front-End (K-chip).
    - We intent to have a Trigger Inhibit logic running on the Front-End electronics (K-chip) which prevents an overflow condition on the PACE. If PACE gets full then LV1A will be blocked until some data has been read out and space is made available.
    - The readout chain gets informed about the trigger gating condition and null events are inserted to maintain readout Synchronization.
- Front-End Readout FIFO (K-chip)
  - Buffer size for lower overflow probability than in the Pipelines
  - Trigger inhibit Logic on the Front-End (on chip)
    - Event Counter is incremented and
    - A null event is inserted which is flagged appropriately.

Readout Synchronization



Front-End (K-chip) can be programmed to send all or some of the following info:

- BC counter to check for clock line miss/bounce pulses
- $EC_{relative}$ counter to check for LV1A line miss/bounce pulses
- PACE col. addr. for pipeline (PACE) synchronization monitoring

Recovery from Readout Synchronization Loss

- Recovery from Loss of Readout Synchronization
  - *The FED detects sync. loss by checking*
    - *the buffer full error flags of the event data packets and*
    - *the time stamps on the event fragments (BC number, Event Number, PACE column addr.)*
  - *Request to Reset the Readout chain.*
    - *Where should be placed this request ?*
- Abort Gap activity
  - *We would like to have the possibility of applying a Front-End electronics reset signal in 1/x abort gaps. The period of reset (x) would depend on the stability of the system.*

Delays associated with Loss of Readout Sync.

FE pipeline (PACE): *Cannot read during a "Reset", Reset takes 1~2 clock cycles*

Dead time = Readout time of stored events in the Pipeline.
For 0 ~ 8 events, Dead time = 0 ~ 50μs

URL Reference

- http://cmsdoc.cern.ch/cms/ECAL/preshower/electronics/synchro/idx.html